64-bit Intel® Xeon™ Processor MP with up to 8MB L3 Cache

Datasheet

March 2005

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Revision History

Version Number	Description	Date
-001	• Initial Release	March 2005

Product Features

- 64-bit Processor with Intel® Extended Memory 64 Technology[1]
- Available at 2.66, 2.83, 3.00, 3.16, 3.33, and 3.66 GHz
- Multi-processing (4 sockets and above) server support
- Binary compatible with applications running on previous members of the Intel® IA-32 microprocessor line
- Intel NetBurst® microarchitecture
- Hyper-Threading Technology
  - — Hardware support for multi-threaded applications
- 667 MHz System bus with data-bus Error Correcting Code (ECC)
  - — Dual independent bus architecture supports two processors per bus segment
  - — Bandwidth up to 5.33 GB/second
  - — Split Transaction Bus with Modified Enhanced Defer improves throughput
- Rapid Execution Engine: Arithmetic Logic Units (ALUs) run at twice the processor core frequency
- Hyper-Pipelined Technology
- Advance Dynamic Execution
  - — Very deep out-of-order execution
  - — Enhanced branch prediction
- Level 1 Execution Trace Cache stores 12 K micro-ops and removes decoder latency from main execution loops
  - — Includes 16-KB Level 1 data cache
- 1MB Advanced Transfer L2 Cache (on-die, full speed Level 2 cache) with 8-way associativity and Error Correcting Code (ECC)
- 4-MB or 8-MB L3 Cache (on-die, full speed Level 3 cache) with 8-way associativity and Error Correcting Code (ECC)
- Enables system support of up to 1024 GB of physical memory
- Streaming SIMD Extensions 2 (SSE2 and SSE3)
  - — 144 new instructions for double-precision floating point operations, media/video streaming, and secure transactions
- Enhanced floating point and multimedia unit for enhanced video, audio, encryption, and 3D performance
- Power Management capabilities
  - — Enhanced Intel Speed-Step® technology
  - — System Management mode
  - — Multiple low-power states
- Advanced System Management Features
  - — System Management Bus
  - — Processor Information ROM (PIROM)
  - — OEM Scratch EEPROM
  - — Thermal Monitor, Thermal Monitor 2 (TM2)
  - — Machine Check Architecture (MCA)
- Execute Disable Bit[2] when used with operating systems helps protect against a certain class of malicious virus attacks.

NOTES:

1. 64-bit Intel® Xeon™ processors with Intel® EM64T requires a computer system with a processor, chipset, BIOS, OS, device drivers and applications enabled for Intel EM64T. Processor will not operate (including 32-bit operation) without an Intel EM64T-enabled BIOS. Performance will vary depending on your hardware and software configurations. Intel EM64T-enabled OS, BIOS, device drivers and applications may not be available. Check with your vendor for more information.
2. Execute Disable Bit requires operating system support. See http://www.intel.com/business/bss/infrastructure/security/xdbit.htm for more information on how to implement this feature.

The 64-bit Intel® Xeon™ processor MP with up to 8MB L3 cache is designed for high-performance multi-processor server applications for mid-tier enterprise serving and server consolidation. Based on the Intel NetBurst® microarchitecture and the new Hyper-Threading Technology, it is binary compatible with previous Intel Architecture (IA-32) processors. The addition of Intel® EM64T provides 64-bit computing and 40-bit addressing provides up to 1 Terabyte of direct memory addressability. The 64-bit Intel® Xeon™ processor MP with 4MB L3 cache is scalable to four processors and beyond in a multiprocessor system providing exceptional performance for applications running on advanced operating systems such as Microsoft Windows* 2003 Server, and Linux* operating systems. The 64-bit Intel® Xeon™ processor MP with 8MB L3 cache delivers compute power at unparalleled value and flexibility for internet infrastructure and departmental server applications, including application servers, databases, and business intelligence. The Intel NetBurst microarchitecture with Hyper-Threading technology and Intel EM64T deliver outstanding performance and headroom for peak internet server workloads, resulting in faster response times, support for more users, and improved scalability.

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1 Introduction

The 64-bit Intel® Xeon™ processor MP with up to 8MB L3 cache is a 64-bit multi-processor capable server processor based on improvements to the Intel NetBurst® microarchitecture. It maintains the tradition of compatibility with IA-32 software and includes features found in the Intel® Xeon™ processor such as Hyper Pipelined Technology, a Rapid Execution Engine, and an Execution Trace Cache. Hyper Pipelined Technology includes a multi-stage pipeline, allowing the processor to reach much higher core frequencies. The 667 MHz front side bus is a quad-pumped bus running off a 166 MHz system clock making 5.3 GB per second data transfer rates possible. The Execution Trace Cache is a level 1 (L1) cache that stores decoded micro-operations, which removes the decoder from the main execution path, thereby increasing performance. In addition, the 64-bit Intel® Xeon™ processor MP with up to 8MB L3 cache includes the Intel® Extended Memory 64 Technology, providing additional address capability.

In addition, enhanced thermal and power management capabilities are implemented, including Thermal Monitor, Thermal Monitor 2 (TM2), and Enhanced Intel SpeedStep® technology. Thermal Monitor and Thermal Monitor 2 provide efficient and effective cooling in high temperature situations. Enhanced Intel SpeedStep technology allows trade-offs to be made between performance and power consumption. This may lower average power consumption (in conjunction with OS support).

The 64-bit Intel® Xeon™ processor MP with up to 8MB L3 cache supports Hyper-Threading Technology. This feature allows a single, physical processor to function as two logical processors. While some execution resources such as caches, execution units, and buses are shared, each logical processor has its own architectural state with its own set of general-purpose registers, control registers to provide increased system responsiveness in multitasking environments, and headroom for next generation multi-threaded applications. More information on Hyper-Threading Technology can be found at http://www.intel.com/technology/hyperthread.

Support for Intel's Execute Disable Bit functionality has been added which can prevent certain classes of malicious “buffer overflow” attacks when combined with a supporting operating system. Execute Disable Bit allows the processor to classify areas in memory by where application code can execute and where it cannot. When a malicious worm attempts to insert code in the buffer, the processor disables code execution, preventing damage or worm propagation.

Other features within the Intel NetBurst microarchitecture include Advanced Dynamic Execution, Advanced Transfer Cache, enhanced floating point and multi-media unit, and Streaming SIMD Extensions 2 (SSE2). The Advanced Dynamic Execution improves speculative execution and branch prediction internal to the processor. The Advanced Transfer Cache is a 1 MB on-die level 2 (L2) cache with increased bandwidth. The floating point and multi-media units include 128-bit wide registers and a separate register for data movement. SSE2 instructions provide highly efficient double-precision floating point, SIMD integer, and memory management operations. In addition, Streaming SIMD Extensions 3 (SSE3) instructions have been added to further extend the capabilities of Intel processor technology. Other processor enhancements include core frequency improvements and microarchitectural improvements.

The 64-bit Intel® Xeon™ processor MP with up to 8MB L3 cache supports Intel® Extended Memory 64 Technology (Intel® EM64T) as an enhancement to Intel’s IA-32 architecture. This enhancement allows the processor to execute operating systems and applications written to take advantage of the 64-bit extension technology. The processor supports 40-bit addressing, data bus

ECC protection (single-bit error correction with double-bit error detection), and the bus protocol addition of the Deferred Phase. Further details can be found in the *64-bit Extension Technology Software Developer's Guide* at http://developer.intel.com/technology/64bitextensions/.

The 64-bit Intel® Xeon™ processor MP with up to 8MB L3 cache is intended for high performance multi-processor server systems with support for up to two processors on a 667 MHz front side bus. The 64-bit Intel® Xeon™ processor MP with up to 8MB L3 cache will be available with 4 MB or 8 MB of on-die level 3 (L3) cache. All versions of the processor will include manageability features. Components of the manageability features include an OEM EEPROM and Processor Information ROM which are accessed through an SMBus interface and contain information relevant to the particular processor and system in which it is installed.

Table 1-1. Features of the 64-bit Intel® Xeon™ Processor MP with up to 8MB L3 Cache

	# of Symmetric Agents	# of Supported Symmetric Agents Per FSB	L2 Advanced Transfer Cache	Integrated L3 Cache	FSB Frequency
Processor	1-255	1 - 2	1 MB	4 MB or 8 MB	667 MHz

The processor is packaged in a 604-pin Flip-Chip Micro Pin Grid Array (FC-mPGA4) package and utilizes a surface-mount Zero Insertion Force (ZIF) mPGA604 socket.

The processor uses a scalable system bus referred to as the "Front Side Bus" (FSB) in this document. The FSB utilizes a split-transaction, deferred reply and modified enhanced deferred phase protocol that improves bandwidth and throughput by reducing the number of cycles needed to return data from a deferred response. The front side bus uses Source-Synchronous Transfer (SST) of address and data to improve performance. The processor transfers data four times per bus clock (4X data transfer rate). Along with the 4X data bus, the address bus can deliver addresses two times per bus clock and is referred to as a 'double-clocked', 'double-pumped', or the 2X address bus. In addition, the Request Phase completes in one clock cycle. Working together, the 4X data bus and 2X address bus provide a data bus bandwidth of up to 5.3 GB per second. Finally, the front side bus is also used to deliver interrupts.

1.1 Terminology

A '#' symbol after a signal name refers to an active low signal, indicating that a signal is in the asserted state when driven to a low level. For example, when RESET# is low (i.e. when RESET# is asserted), a reset has been requested. Conversely, when NMI is high (i.e. when NMI is asserted), a nonmaskable interrupt request has occurred. In the case of signals where the name does not imply an active state but describes part of a binary sequence (such as *address* or *data*), the '#' symbol implies that the signal is inverted. For example, D[3:0] = 'HLHL' refers to a hex 'A', and D[3:0]# = 'LHLH' also refers to a hex 'A' (H= High logic level, L= Low logic level).

"Front side bus" refers to the interface between the processor, system core logic (i.e. the chipset components), and other bus agents. The front side bus supports multiprocessing and cache coherency. For this document, "front side bus" is used as the generic term for the processor system bus.

Commonly used terms are explained here for clarification:

- **64-bit Intel® Xeon™ processor MP with up to 8MB L3 cache** — The entire product, including processor core substrate and integrated heat spreader (IHS).

- **Enhanced Intel SpeedStep technology** — Enhanced Intel SpeedStep technology is the next generation implementation of the Geyserville technology which extends power management capabilities of servers.
- **FC-mPGA4** — The processor is available in a Flip-Chip Micro Pin Grid Array 4 package, consisting of a processor core mounted on a pinned substrate with an integrated heat spreader (IHS). This packaging technology employs a 1.27 mm [0.05 in] pitch for the substrate pins.
- **Front Side Bus (FSB)** — The electrical interface that connects the processor to the chipset. Also referred to as the processor system bus or the system bus. All memory and I/O transactions as well as interrupt messages pass between the processor and chipset over the FSB.
- **Functional Operation** — Refers to the normal operating conditions in which all processor specifications, including DC, AC, system bus, signal quality, mechanical, and thermal, are satisfied.
- **Integrated Heat Spreader (IHS)** — A component of the processor package used to enhance the thermal performance of the package. Component thermal solutions interface with the processor at the IHS surface.
- **mPGA604** — The processor mates with the system board through this surface mount, 604-pin, zero insertion force (ZIF) socket.
- **OEM** — Original Equipment Manufacturer.
- **Processor core** — The processor's execution engine. All AC timing and signal integrity specifications are to the pads of the processor core.
- **Processor Information ROM (PIROM)** — A memory device located on the processor and accessible via the System Management Bus (SMBus) which contains information regarding the processor's features. This device is shared with the Scratch EEPROM, is programmed during manufacturing, and is write-protected.
- **Scratch EEPROM (Electrically Erasable, Programmable Read-Only Memory)** — A memory device located on the processor and addressable via the SMBus which can be used by the OEM to store information useful for system management.
- **SMBus** — System Management Bus. A two-wire interface through which simple system and power management related devices can communicate with the rest of the system. It is based on the principals of the operation of the I^2C* two-wire serial bus from Phillips Semiconductor.

  Note: I^2C is a two-wire communications bus/protocol developed by Philips. SMBus is a subset of the I^2C bus/protocol and was developed by Intel. Implementations of the I^2C bus/protocol or the SMBus bus/protocol may require licenses from various entities, including Philips Electronics N.V. and North American Philips Corporation.
- **Storage Conditions** — Refers to a non-operational state. The processor may be installed in a platform, in a tray, or loose. Processors may be sealed in packaging or exposed to free air. Under these conditions, processor pins should not be connected to any supply voltages, have any I/Os biased, or receive any clocks.
- **Symmetric Agent** - A symmetric agent is a processor which shares the same I/O subsystem and memory array, and runs the same operating system as another processor in a system. Systems using symmetric agents are known as Symmetric MultiProcessing (SMP) systems. The 64-bit Intel® Xeon™ processor MP with up to 8MB L3 cache should only be used in SMP systems which have two or fewer symmetric agents per front side bus.

1.2 References

Material and concepts available in the following documents may be beneficial when reading this document. Some document references in this specification are generic and should be referenced back to the specific documents listed here.

Document	Intel Order Number	Notes
AP-485 Intel® Processor Identification and the CPUID Instruction	241618	2
ATX/ATX12V Power Supply Design Guidelines		3
Chassis Strength and Stiffness Measurement and Improvement Guidelines for Direct Chassis Attach Solutions		1
IA-32 Intel® Architecture and Intel® Extended Memory 64 Technology Software Developer's Manual Documentation Changes	252046	2
IA-32 Intel® Architecture Optimization Reference Manual	248966	2
IA-32 Intel® Architecture Software Developer's Manual • Volume 1: Basic Architecture • Volume 2A: Instruction Set Reference, A-M • Volume 2B: Instruction Set Reference, N-Z • Volume 3: System Programming Guide	 253665 253666 253667 253668	2
Intel® Extended Memory 64 Technology Software Developer's Manual • Volume 1 • Volume 2	 300834 300835	2
mPGA604 Socket Design Guidelines	254239	1
MPS Power Supply: A Server System Infrastructure (SSI) Specification For Midrange Chassis Power Supplies		4
64-bit Intel® Xeon™ Processor MP with up to 8MB L3 Cache Specification Update	289741	1
64-bit Intel® Xeon™ processor MP with up to 8MB L3 Cache Mechanical Models		1
64-bit Intel® Xeon™ processor MP with up to 8MB L3 Cache Cooling Solution Mechanical Models		1
64-bit Intel® Xeon™ processor MP with up to 8MB L3 Cache Thermal Test Vehicle and Cooling Solution Thermal Models		1
64-bit Intel® Xeon™ Processor MP with up to 8MB L3 Cache Thermal/Mechanical Design Guide	306749	1
Prescott New Instructions Software Development Guide	252490	2
System Management Bus (SMBus) Specification		5
Voltage Regulator Module (VRM) and Enterprise Voltage Regulator Down (EVRD) 10.1 Design Guidelines	302732	1
Voltage Regulator Module (VRM) and Enterprise Voltage Regulator Down (EVRD) 10.2 Design Guidelines	306760	1
Voltage Regulator Module (VRM) 10.2L Design Guidelines	306761	1
VRM 9.1 DC-DC Converter Design Guidelines	306760	2

NOTES:
1. See the *Intel® Xeon™ Processor Message of the Week* for latest document version and order numbers. Contact your Intel representative to receive the latest revisions of these documents.
2. This collateral is available publicly at http://developer.intel.com.
3. This document is available at http://www.formfactors.org.

4. This document is available at http://www.ssiforum.org.
5. This document is available at http://www.smbus.org.

1.3 State of Data

The data contained within this document is subject to change. It is the most accurate information available by the publication date of this document. Electrical AC / DC specifications are based on I/O buffer behavior in the production processor. Mechanical data is based on the final FC-mPGA4 package design.

For processor stepping information, refer to the *64-bit Intel® Xeon™ Processor MP with up to 8MB L3 Cache Specification Update*.

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2 Electrical Specifications

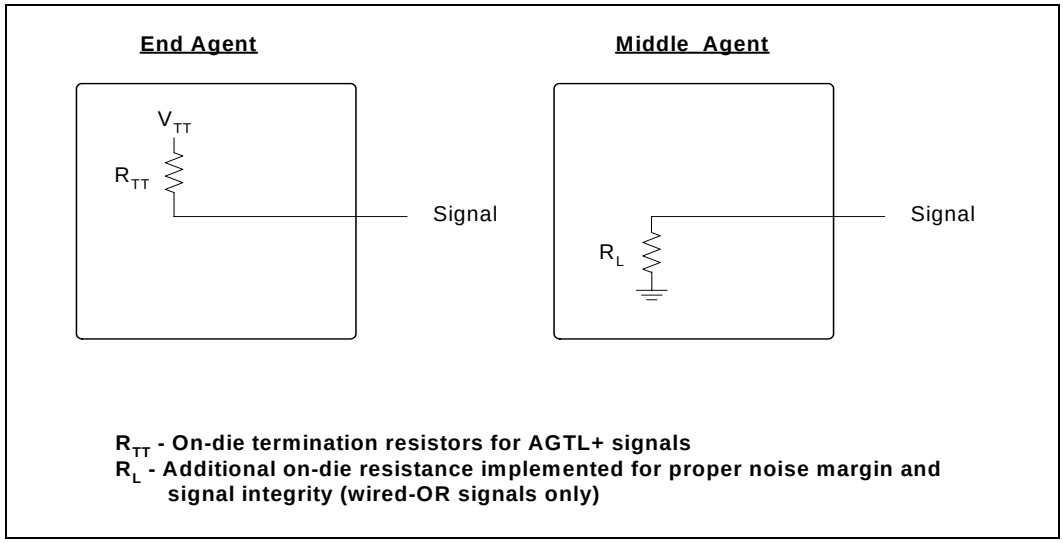
2.1 Front Side Bus and GTLREF

Most processor front side bus (FSB) signals use Assisted Gunning Transceiver Logic (AGTL+) signaling technology. This technology provides improved noise margins and reduced ringing through low voltage swings and controlled edge rates. AGTL+ buffers are open-drain and require pull-up resistors to provide the high logic level and termination. AGTL+ output buffers differ from GTL+ buffers with the addition of an active pMOS pull-up transistor to “assist” the pull-up resistors during the first clock of a low-to-high voltage transition. Platforms implement a termination voltage level for AGTL+ signals defined as V_{TT}. Because platforms implement separate power planes for each processor, separate V_{CC} and V_{TT} supplies are necessary. This configuration allows for improved noise tolerance as processor frequency increases. Speed enhancements to data and address busses have caused signal integrity considerations and platform design methods to become even more critical than with previous processor families.

The AGTL+ inputs require a reference voltage (GTLREF) which is used by the receivers to determine if a signal is a logical 0 or a logical 1. GTLREF must be generated on the motherboard (see Table 2-19 for GTLREF specifications). The on-die termination resistors are a selectable feature and can be enabled or disabled via the ODTEN signal. For end bus agents, on-die termination resistors are enabled to control reflections on the transmission line. For the middle bus agent, on-die termination R_{TT} resistors must be disabled. Intel chipsets will also provide on-termination, thus eliminating the need to terminate the bus on the motherboard for most AGTL+ signals. Processor wired-OR signals may also include additional on-die resistors (R_L) to further ensure proper noise margin and signal integrity. R_L is not configurable and is always enabled for these signals. See Table 2-6 for a list of these signals.

Figure 2-1 illustrates the active on-die termination.

Figure 2-1. On-Die Front Side Bus Termination



Note: Some AGTL+ signals do not include on-die termination (R_{TT}) and must be terminated on the motherboard. See Table 2-6 for details regarding these signals.

2.1.1 Front Side Bus Clock and Processor Clocking

BCLK[1:0] directly controls the front side bus interface speed as well as the core frequency of the processor. The processor core frequency is a multiple of the BCLK[1:0] frequency. The processor bus ratio multiplier will be set at its default ratio during manufacturing. The default setting generates the maximum speed for the processor. It is possible to override this setting using software. Refer to the Processor BIOS Writers Guide for details. This will permit operation at a speed lower than the processor's tested frequency.

The processor core frequency is configured during reset by using values stored internally during manufacturing. The stored values set the highest bus fraction at which the particular processor can operate. If lower speeds are desired, the appropriate bus ratio multiplier can be configured by driving the A[21:16]# pins at reset. For details of operation at core frequencies lower than the maximum rated processor speed, refer to the Processor BIOS Writers Guide.

The bus ratio multipliers supported are shown in Table 2-1. Other combinations will not be validated or supported by Intel. For a given processor, only the ratios which result in a core frequency equal to or less than the frequency marked on the processor are supported.

Table 2-1. Core Frequency to Front Side Bus Multiplier Configuration

Core Frequency to Front Side Bus Multiplier	Core Frequency	A21#	A20#	A19#	A18#	A17#	A16#
1/16	2.66 GHz	L	H	L	L	L	L
1/17	2.83 GHz	L	H	L	L	L	H
1/18	3.00 GHz	L	H	L	L	H	L
1/19	3.16 GHz	L	H	L	L	H	H
1/20	3.33 GHz	L	H	L	H	L	L
1/22	3.66 GHz	L	H	L	H	H	L

NOTES:
1. Individual processors operate only at or below the frequency marked on the package.
2. Listed frequencies are not necessarily committed production frequencies.
3. For valid core frequencies of the processor, refer to the Processor Specification Update.
4. As described in Section 1.1, "H" refers to a high logic level (i.e. signal asserted) and "L" refers to a low logic level (i.e. signal deasserted).

The processor uses a differential clocking implementation.

2.1.2 Front Side Bus Clock Select (BSEL[1:0])

The BSEL[1:0] signals are used to select the frequency of the processor input clock (BCLK[1:0]). Table 2-2 defines the possible combinations of the signals and the frequency associated with each combination. The required frequency is determined by the processor, chipset, and clock synthesizer. All processors must operate at the same front side bus frequency.

The processor operates at a 667 MHz front side bus frequency (selected by a 166 MHz BCLK[1:0] frequency). Individual processors operate at the front side bus frequency specified by BSEL[1:0].

For more information about these pins, refer to Section 6.1.

Table 2-2. BSEL[1:0] Frequency Table for BCLK[1:0]

BSEL1	BSEL0	Function
0	0	RESERVED
0	1	RESERVED
1	0	RESERVED
1	1	166 MHz

2.1.3 Phase Lock Loop (PLL) Power and Filter

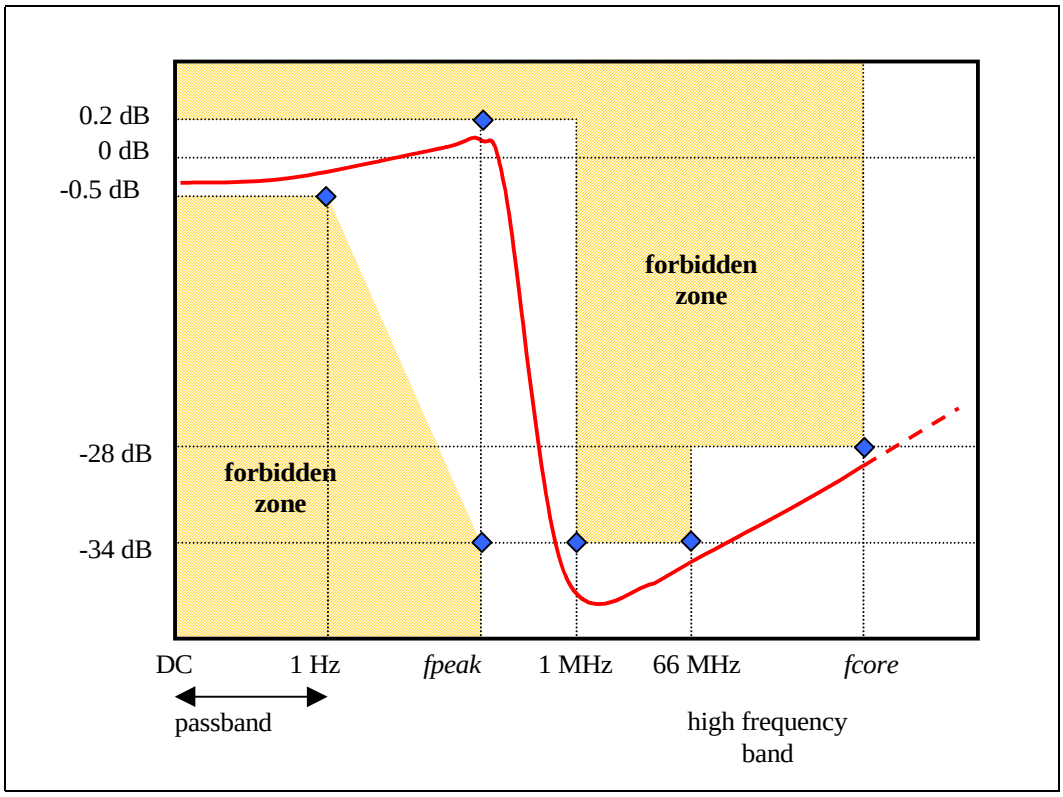
V_{CCA}, $V_{CCIOPLL}$, and V_{CCA_CACHE} are power sources required by the PLL clock generators on the processor. These are analog PLLs and they require low noise power supplies for minimum jitter. These supplies must be low pass filtered from V_{TT}.

The AC low-pass requirements, with input at V_{TT}, are as follows:

- < 0.2 dB gain in pass band
- < 0.5 dB attenuation in pass band < 1 Hz
- > 34 dB attenuation from 1 MHz to 66 MHz
- > 28 dB attenuation from 66 MHz to core frequency

The filter requirements are illustrated in Figure 2-2.

Figure 2-2. Phase Lock Loop (PLL) Filter Requirements



NOTES:
1. Diagram not to scale.
2. No specification for frequencies beyond f_{core} (core frequency).
3. f_{peak}, if existent, should be less than 0.05MHz.
4. f_{core} represents the maximum core frequency supported by the platform.

2.2 Voltage Identification (VID)

The VID[5:0] pins supply the encodings that determine the voltage to be supplied by the V_{CC} (the core voltage for the processor) voltage regulator. The VID specification for the processor is defined by the *Voltage Regulator Module (VRM) and Enterprise Voltage Regulator-Down (EVRD) 10.1 Design Guidelines*, the *Voltage Regulator Module (VRM) and Enterprise Voltage Regulator-Down (EVRD) 10.2 Design Guidelines*, and the *Voltage Regulator Module (VRM) 10.2L Design Guidelines*. Please refer to these documents for all VRM and VRD design issues. The voltage set by the VID signals is the maximum V_{CC} voltage allowed by the processor. VID signals are open drain outputs, which must be pulled up to V_{TT}. Please refer to Table 2-13 for the DC specifications for these signals. A minimum V_{CC} voltage is provided in Table 2-9 and changes with frequency. This allows processors running at a higher frequency to have a relaxed minimum V_{CC} voltage specification. The specifications have been set such that one voltage regulator can work with all supported frequencies.

Individual processor VID values may be calibrated during manufacturing such that two devices at the same core speed may have different default VID settings. Furthermore, any processor, even those on the same processor front side bus, can drive different VID settings during normal operation.

The processor uses six voltage identification pins, VID[5:0], to support automatic selection of power supply voltages. Table 2-3 specifies the voltage level corresponding to the state of VID[5:0]. A '1' in this table refers to a high voltage level and a '0' refers to a low voltage level. If the processor socket is empty (i.e. VID[5:0] = x11111), or the voltage regulation circuit cannot supply the voltage that is requested, the processor's voltage regulator must disable itself.

The processor provides the ability to operate while transitioning to an adjacent VID and its associated processor core voltage (V_{CC}). This will represent a DC shift in the load line. It should be noted that a low-to-high or high-to-low voltage state change may result in as many VID transitions as necessary to reach the target core voltage. Transitions above the specified VID are not permitted. Table 2-9 includes VID step sizes and DC shift ranges. Minimum and maximum voltages must be maintained as shown in Table 2-10 and Figure 2-4.

The VRM or VRD utilized must be capable of regulating its output to the value defined by the new VID. DC specifications for VID transitions are included in Table 2-9 and Table 2-10.

Power source characteristics must be guaranteed to be stable whenever the supply to the voltage regulator is stable.

Table 2-3. Voltage Identification (VID) Definition

VID5	VID4	VID3	VID2	VID1	VID0	VID (V)		VID5	VID4	VID3	VID2	VID1	VID0	VID (V)
0	0	1	0	1	0	0.8375		0	1	1	0	1	0	1.2125
1	0	1	0	0	1	0.8500		1	1	1	0	0	1	1.2250
0	0	1	0	0	1	0.8625		0	1	1	0	0	1	1.2375
1	0	1	0	0	0	0.8750		1	1	1	0	0	0	1.2500
0	0	1	0	0	0	0.8875		0	1	1	0	0	0	1.2625
1	0	0	1	1	1	0.9000		1	1	0	1	1	1	1.2750
0	0	0	1	1	1	0.9125		0	1	0	1	1	1	1.2875
1	0	0	1	1	0	0.9250		1	1	0	1	1	0	1.3000
0	0	0	1	1	0	0.9375		0	1	0	1	1	0	1.3125
1	0	0	1	0	1	0.9500		1	1	0	1	0	1	1.3250
0	0	0	1	0	1	0.9625		0	1	0	1	0	1	1.3375
1	0	0	1	0	0	0.9750		1	1	0	1	0	0	1.3500
0	0	0	1	0	0	0.9875		0	1	0	1	0	0	1.3625
1	0	0	0	1	1	1.0000		1	1	0	0	1	1	1.3750
0	0	0	0	1	1	1.0125		0	1	0	0	1	1	1.3875
1	0	0	0	1	0	1.0250		1	1	0	0	1	0	1.4000
0	0	0	0	1	0	1.0375		0	1	0	0	1	0	1.4125
1	0	0	0	0	1	1.0500		1	1	0	0	0	1	1.4250
0	0	0	0	0	1	1.0625		0	1	0	0	0	1	1.4375
1	0	0	0	0	0	1.0750		1	1	0	0	0	0	1.4500
0	0	0	0	0	0	1.0875		0	1	0	0	0	0	1.4625
1	1	1	1	1	1	VRM off		1	0	1	1	1	1	1.4750
0	1	1	1	1	1	VRM off		0	0	1	1	1	1	1.4875
1	1	1	1	1	0	1.1000		1	0	1	1	1	0	1.5000
0	1	1	1	1	0	1.1125		0	0	1	1	1	0	1.5125
1	1	1	1	0	1	1.1250		1	0	1	1	0	1	1.5250
0	1	1	1	0	1	1.1375		0	0	1	1	0	1	1.5375
1	1	1	1	0	0	1.1500		1	0	1	1	0	0	1.5500
0	1	1	1	0	0	1.1625		0	0	1	1	0	0	1.5625
1	1	1	0	1	1	1.1750		1	0	1	0	1	1	1.5750
0	1	1	0	1	1	1.1875		0	0	1	0	1	1	1.5875
1	1	1	0	1	0	1.2000		1	0	1	0	1	0	1.6000

2.3 Cache Voltage Identification (CVID)

The CVID[3:0] pins supply the encodings that determine the voltage to be supplied by the V_{CACHE} (the L3 cache voltage for the processor) voltage regulator. The CVID specification for the processor is defined by the *VRM 9.1 DC-DC Converter Design Guidelines*, *Voltage Regulator Module (VRM) and Enterprise Voltage Regulator-Down (EVRD) 10.1 Design Guidelines*, *Voltage Regulator Module (VRM) and Enterprise Voltage Regulator-Down (EVRD) 10.2 Design Guidelines*, and *Voltage Regulator Module (VRM)10.2L Design Guidelines*. The voltage set by the CVID pins is the maximum V_{CACHE} voltage allowed by the processor. A minimum V_{CACHE} voltage is provided in Table 2-9.

Processors with the same front side bus frequency, internal cache sizes, and stepping will have consistent CVID values.

The processor uses four voltage identification pins (CVID[3:0]) to support automatic selection of power supply voltages. Table 2-4 specifies the voltage level corresponding to the state of CVID[3:0]. A ‘1’ in this table refers to a high voltage level and a ‘0’ refers to a low voltage level. If the processor socket is empty, or the voltage regulation circuit cannot supply the voltage that is requested, the processor’s voltage regulator must disable itself.

Table 2-4. Cache Voltage Identification (CVID) Definition

CVID3	CVID2	CVID1	CVID0	CVID (V)
1	1	1	1	Off
1	1	1	0	1.100
1	1	0	1	1.125
1	1	0	0	1.150
1	0	1	1	1.175
1	0	1	0	1.200
1	0	0	1	1.225
1	0	0	0	1.250
0	1	1	1	1.275
0	1	1	0	1.300
0	1	0	1	1.325
0	1	0	0	1.350
0	0	1	1	1.375
0	0	1	0	1.400
0	0	0	1	1.425
0	0	0	0	1.450

NOTE: The voltage regulator will have a fifth VID input and, for VRM 10.2-compliant regulators, a sixth VID input as well. The extra input(s) should be tied to a high voltage on the motherboard for correct operation.

2.4 Reserved, Unused, and TESTHI Pins

All RESERVED pins must be left unconnected. Connection of these pins to V_{CC}, V_{SS}, or to any other signal (including each other) can result in component malfunction or incompatibility with future processors. See Section 5 for a pin listing for the processor and the location of all RESERVED pins.

For reliable operation, always terminate unused inputs or bidirectional signals to their respective deasserted states. On-die termination has been included on the processor to allow signals to be terminated within the processor silicon. Most unused AGTL+ inputs may be left as no-connects since AGTL+ termination is provided on the processor silicon. See Table 2-6 for details on AGTL+ signals that do not include on-die termination. Unused active-high inputs should be connected through a resistor to ground (V_{SS}). Unused outputs may be left unconnected. However, this may interfere with some TAP functions, complicate debug probing, and prevent boundary scan testing. A resistor must be used when tying bidirectional signals to power or ground. When tying any signal to power or ground, a resistor will also allow for system testability. For unused AGTL+ input or I/O signals, use pull-up resistors of the same value as the on-die termination resistors (R_{TT}). See Table 2-15.

Most TAP signals, GTL+ asynchronous inputs, and GTL+ asynchronous outputs do not include on-die termination (see Table 2-6 for those signals which do not have on-die termination). Inputs and used outputs must be terminated on the system board. Unused outputs may be terminated on the system board or left connected. Note that leaving unused outputs unterminated may interfere with some TAP functions, complicate debug probing, and prevent boundary scan testing.

The TESTHI pins should be tied to V_{TT} using a matched resistor, where a matched resistor has a resistance value within ±20% of the impedance of the board transmission line traces. For example, if the trace impedance is 50 W, then a value between 40 W and 60 W is required.

The TESTHI pins may use individual pull-up resistors or be grouped together as detailed below. Please note that utilization of boundary scan test will not be functional if pins are connected together. A matched resistor should be used for each group:

- TESTHI[3:0]
- TESTHI[6:5]
- TESTHI4 — cannot be grouped with other TESTHI signals

2.5 Mixing Processors

Intel supports and validates multi-processor configurations in which all processors operate with the same front side bus frequency and internal cache sizes. Intel does not support or validate operation of processors with different cache sizes. Mixing different processor steppings but the same model (as per the CPUID instruction) is supported. Details on CPUID are provided in the Processor BIOS Writers Guide document and the *AP-485 Intel® Processor Identification and the CPUID Instruction* application note.

2.6 Front Side Bus Signal Groups

The front side bus signals are grouped by buffer type as listed in Table 2-5. The buffer type indicates which AC and DC specifications apply to the signals. AGTL+ input signals have differential input buffers that use GTLREF as a reference level. In this document, the term "AGTL+ Input" refers to the AGTL+ input group as well as the AGTL+ I/O group when receiving. Similarly, "AGTL+ Output" refers to the AGTL+ output group as well as the AGTL+ I/O group when driving. AGTL+ asynchronous outputs can become active anytime and include an active pMOS pull-up transistor to assist during the first clock of a low-to-high voltage transition.

Implementing a source synchronous data bus requires specifying two sets of timing parameters. One set is for common clock signals which are dependent upon the rising edge of BCLK0 (ADS#, HIT#, HITM#, etc.). The second set is for the source synchronous signals that are relative to their respective strobe lines (data and address) as well as the rising edge of BCLK0. Asynchronous signals are present (A20M#, IGNNE#, etc.) and can become active at any time during the clock cycle. Table 2-5 identifies signals as common clock, source synchronous, and asynchronous.

Table 2-5. Front Side Bus Pin Groups (Sheet 1 of 2)

Signal Group	Type	Signals[1]
AGTL+ Common Clock Input	Synchronous to BCLK[1:0]	BPRI#, BR[3:1]#, DEFER#, ID[7:0]#, IDS#, OOD#, RESET#, RS[2:0]#, RSP#, TRDY#
AGTL+ Common Clock I/O	Synchronous to BCLK[1:0]	ADS#, AP[1:0]#, BINIT#, BNR#, BPM[5:0]#, BR0#, DBSY#, DP[3:0]#, DRDY#, HIT#, HITM#, LOCK#, MCERR#
AGTL+ Source Synchronous I/O	Synchronous to associated strobe	**Signals** / **Associated Strobe**: REQ[4:0]#, A[37:36,16:3]# / ADSTB0# A[39:38,35:17]# / ADSTB1# D[15:0]#, DEP[1:0]#, DBI0# / DSTBP0#, DSTBN0# D[31:16]#, DEP[3:2]#, DBI1# / DSTBP1#, DSTBN1# D[47:32]#, DEP[5:4]#, DBI2# / DSTBP2#, DSTBN2# D[63:48]#, DEP[7:6]#, DBI3# / DSTBP3#, DSTBN3#
AGTL+ Strobe Input/Output	Synchronous to BCLK[1:0]	ADSTB[1:0]#, DSTBP[3:0]#, DSTBN[3:0]#
AGTL+ Asynchronous Output	Asynchronous	FERR#/PBE#, IERR#, PROCHOT#
GTL+ Asynchronous Input	Asynchronous	A20M#, FORCEPR#, IGNNE#, INIT#, LINT0/ INTR, LINT1/NMI, SMI#, STPCLK#
GTL+ Asynchronous Output	Asynchronous	THERMTRIP#
TAP Input	Synchronous to TCK	TCK, TDI, TMS
TAP Input	Asynchronous	TRST#
TAP Output	Synchronous to TCK	TDO

Table 2-5. Front Side Bus Pin Groups (Sheet 2 of 2)

Signal Group	Type	Signals[1]
Front Side Bus Clock Input	Clock	BCLK[1:0]
SMBus	Synchronous to SM_CLK	SM_ALERT#, SM_CLK, SM_DAT, SM_EP_A[2:0], SM_TS_A[1:0], SM_WP
Power/Other	Power/Other	BOOT_SELECT, BSEL[1:0], COMP0, CVID[3:0], GTLREF[3:0], ODTEN, PWRGOOD, RESERVED, SKTOCC#, SLEW_CTRL, SM_VCC, TEST_BUS, TESTHI[6:0], V_{CACHE}, V_{CC}, V_{CCA}, V_{CCA_CACHE}, $V_{CC\_CACHE\_SENSE}$, $V_{CCIOPLL}$, V_{CCPLL}, $V_{CCSENSE}$, VID[5:0], VIDPWRGD, V_{SS}, V_{SSA}, V_{SSA_CACHE}, $V_{SS\_CACHE\_SENSE}$, $V_{SSSENSE}$, V_{TT}, VTTEN

NOTES:
1. Refer to Section 6.1 for signal descriptions.

Table 2-6. Signal Description Table

Signals with R_{TT}[1]
A[39:3]#, ADS#, ADSTB[1:0]#, AP[1:0]#, BINIT#, BNR#, BOOT_SELECT[2], BPRI#, D[63:0]#, DBI[3:0]#, DBSY#, DEFER#, DEP[7:0]#, DP[3:0]#, DRDY#, DSTBN[3:0]#, DSTBP[3:0]#, HIT#, HITM#, ID[7:0]#, IDS#, LOCK#, MCERR#, OOD#, REQ[4:0]#, RS[2:0]#, RSP#, TRDY#
Signals with R_L
BINIT#, BNR#, HIT#, HITM#, MCERR#

NOTES:
1. Signals not included in the "Signals with R_{TT}" list require termination on the baseboard. Please refer to Table 2-5 for the signal type and Table 2-13 to Table 2-18 for the corresponding DC specifications.
2. The BOOT_SELECT pin is not terminated to R_{TT}. It has a 500-5000 Ω internal pullup.

The ODTEN signals enables or disables R_{TT}. Those signals affected by ODTEN still present R_{TT} termination to the signal's pin when the processor is placed in tri-state mode.

Furthermore, the following signals are not affected when the processor is placed in tri-state mode: BSEL[1:0], CVID[3:0], SKTOCC#, SM_ALERT#, SM_CLK, SM_DAT, SM_EP_A[2:0], SM_TS_A[1:0], SM_WP, TEST_BUS, TESTHI[6:0], VID[5:0], and VTTEN.

Table 2-7. Signal Reference Voltages

GTLREF	V_{TT} / 2
A20M#, A[39:3]#, ADS#, ADSTB[1:0]#, AP[1:0]#, BINIT#, BNR#, BPM[5:0]#, BPRI#, BR[3:0]#, D[63:0]#, DBI[3:0]#, DBSY#, DEFER#, DEP[7:0]#, DP[3:0]#, DRDY#, DSTBN[3:0]#, DSTBP[3:0]#, FORCEPR#, HIT#, HITM#, ID[7:0]#, IDS#, IGNNE#, INIT#, LINT0/INTR, LINT1/NMI, LOCK#, MCERR#, ODTEN, OOD#, REQ[4:0]#, RESET#, RS[2:0]#, RSP#, SMI#, STPCLK#, TRDY#	BOOT_SELECT, PWRGOOD[1], TCK[1], TDI[1], TMS[1], TRST#[1], VIDPWRGD

NOTES:
1. These signals also have hysteresis added to the reference voltage. See Table 2-16 for more information.

2.7 GTL+ Asynchronous and AGTL+ Asynchronous Signals

The processor does not utilize CMOS voltage levels on any signals that connect to the processor silicon. As a result, inputs signals such as A20M#, FORCEPR#, IGNNE#, INIT#, LINT0/INTR, LINT1/NMI, SMI#, and STPCLK# utilize GTL buffers. Legacy output THERMTRIP# utilizes a GTL+ output buffer. All of these asynchronous signals follow the same DC requirements as GTL+ signals; however, the outputs are not driven high (during the logical 0-to-1 transition) by the processor. FERR#/PBE#, IERR#, and PROCHOT# have now been defined as AGTL+ asynchronous signals as they include an active pMOS device. GTL+ asynchronous and AGTL+ asynchronous signals do not have setup or hold time specifications in relation to BCLK[1:0]. However, all of the GTL+ asynchronous and AGTL+ asynchronous signals are required to be asserted/deasserted for at least six BCLKs in order for the processor to recognize the proper signal state, except during power-on configuration (see Table 2-24 for the proper specifications at RESET). See Table 2-17 and Table 2-23 for the DC and AC specifications for the GTL+ asynchronous and AGTL+ asynchronous signal groups.

2.8 Test Access Port (TAP) Connection

Due to the voltage levels supported by other components in the TAP logic, Intel recommends that the processor(s) be first in the TAP chain, followed by any other components within the system. Use of a translation buffer to connect to the rest of the chain is recommended unless one of the other components is capable of accepting an input of the appropriate voltage. Similar considerations must be made for TCK, TMS, TRST#, TDI, and TDO. Two copies of each signal may be required, each driving a different voltage level.

2.9 Maximum Ratings

Table 2-8 specifies absolute maximum and minimum ratings. Within functional operation limits, functionality and long-term reliability can be expected.

At conditions outside functional operation condition limits, but within absolute maximum and minimum ratings, neither functionality nor long-term reliability can be expected. If a device is returned to conditions within functional operation limits after having been subjected to conditions outside these limits, but within the absolute maximum and minimum ratings, the device may be functional, but with its lifetime degraded depending on exposure to conditions exceeding the functional operation condition limits.

At conditions exceeding absolute maximum and minimum ratings, neither functionality nor long-term reliability can be expected. Moreover, if a device is subjected to these conditions for any length of time then, when returned to conditions within the functional operating condition limits, it will either not function, or its reliability will be severely degraded.

Although the processor contains protective circuitry to resist damage from static electric discharge, precautions should always be taken to avoid high static voltages or electric fields.

Table 2-8. Processor Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Notes[1,2]
V_{CC}	Processor core supply voltage with respect to Vss	-0.3	1.55	V	
V_{CACHE}	Processor L3 cache voltage with respect to Vss	-0.3	1.55	V	
V_{TT}	Front side bus termination voltage with respect to Vss	-0.3	1.55	V	
T_{CASE}	Processor case temperature	See Section 7	See Section 7	°C	
$T_{STORAGE}$	Processor storage temperature	-40	85	°C	3, 4

NOTES:
1. For functional operation, all processor electrical, signal quality, mechanical, and thermal specifications must be satisfied.
2. Overshoot and undershoot voltage guidelines for input, output, and I/O signals are outlined in Section 3. Excessive overshoot or undershoot on any signal will likely result in permanent damage to the processor.
3. Storage temperature is applicable to storage conditions only. In this scenario, the processor must not receive a clock, and no pins can be connected to a voltage bias. Storage within these limits will not affect the long-term reliability of the device. For functional operation, please refer to the processor case temperature specifications.
4. This rating applies to the processor and does not include any packaging or trays.

2.10 Processor DC Specifications

The following notes apply:

- The processor DC specifications in this section are defined at the processor core silicon and not at the package pins unless noted otherwise.
- The notes associated with each parameter are part of the specification for that parameter.
- Unless otherwise noted, all specifications in the tables apply to all frequencies and cache sizes.
- Unless otherwise noted, all the specifications in the tables are based on estimates and simulations. These specifications will be updated with characterized data from silicon measurements at a later date.

See Section 6 for the pin signal definitions. Most of the signals on the processor front side bus are in the AGTL+ signal group. The DC specifications for these signals are listed in Table 2-15.

Table 2-9 through Table 2-18 list the DC specifications for the processor and are valid only while meeting specifications for case temperature, clock frequency, and input voltages.

2.10.1 Flexible Motherboard (FMB) Guidelines

The FMB guidelines are estimates of the maximum values that the processor will have over certain time periods. The values are only estimates as actual specifications for future processors may differ. The processor may or may not have specifications equal to the FMB value in the foreseeable future. System designers should meet the FMB values to ensure that their systems will be compatible with future releases of the processor.

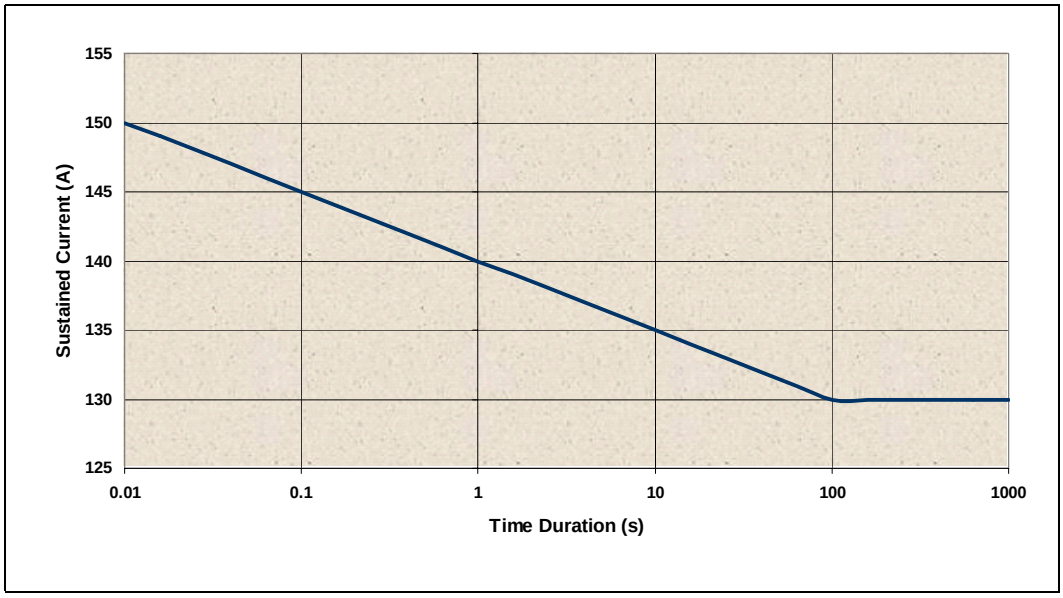
Table 2-9. Voltage and Current Specifications

Symbol	Parameter	Core Freq	Min	Typ	Max	VID	Unit	Notes
V_{CC}	V_{CC} for processor core	FMB	Refer to Table 2-10			1.3875	V	1,2,3, 4,5,7
VID Transition	VID step size during transition	All freq.				± 12.5	mV	18
	Total allowable DC load line shift from VID steps	All freq.				450	mV	19
V_{CACHE}	V_{CC} for processor L3 cache	All freq.	1.125		CVID	1.275	V	17
V_{TT}	FSB termination voltage (DC specification)	All freq.	1.176	1.20	1.224		V	11,12, 13
V_{TT}	FSB termination voltage (AC specification)	All freq.	1.140	1.20	1.260		V	11,12, 13,14
SM_VCC	SMBus supply voltage	All freq.	3.135	3.300	3.465		V	13
I_{CC}	I_{CC} for processor core	FMB			91		A	7,10
I_{CC_TDC}	Thermal Design Current (TDC)	FMB			86		A	20
I_{CACHE}	I_{CC} for processor L3 cache	All freq			24		A	
I_{TT}	FSB termination current, post power good	All freq.			4		A	11,15,21
I_{TT}	FSB mid-agent current, post power good	All freq.			1.3		A	11,16,21
I_{SM_VCC}	I_{CC} for SMBus supply	All freq.		100	122.5		mA	11
I_{SGnt_CORE}	I_{CC} Stop-Grant Core	All freq.			56		A	6,9
I_{SGnt_CACHE}	I_{CC} Stop-Grant Cache	All freq.			23		A	6,9
I_{TCC}	I_{CC} TCC active	All freq.			I_{CC}		A	8
$I_{CC\ VCCA}$	I_{CC} for PLL pin	All freq.			60		mA	
$I_{CC\ VCCIOPLL}$	I_{CC} for I/O PLL pin	All freq.			60		mA	
$I_{CC\ VCCA\_CACHE}$	I_{CC} for L3 cache PLL pin	All freq.			60		mA	
$I_{CC\ GTLREF}$	I_{CC} per GTLREF pin	All freq.			200		µA	

NOTES:
1. These voltages and frequencies are targets only. A variable voltage source should exist on systems in the event that a different voltage is required. See Section 2.2 and Table 2-3 for more information.
2. The voltage specification requirements are measured across the $V_{CCSENSE}$ and $V_{SSSENSE}$ pins using an oscilloscope set to a 100 MHz bandwidth and probes that are 1.5 pF maximum capacitance and 1 MΩ minimum impedance at the processor socket. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled into the scope probe.
3. Refer to Table 2-10 for the minimum, typical, and maximum V_{CC} allowed for a given current. The processor should not be subjected to any V_{CC} and I_{CC} combination wherein V_{CC} exceeds V_{CC_MAX} for a given current.
4. Moreover, V_{CC} should never exceed the VID voltage. Failure to adhere to this specification can shorten the processor lifetime.
5. V_{CC_MIN} and V_{CC_MAX} are defined at the frequency's associated I_{CC_MAX} on the V_{CC} load line.
6. The current specified is also for the HALT State.
7. FMB is the Flexible Motherboard guideline. These guidelines are for estimation purposes only. See Section 2.10.1 for further details on FMB guidelines.
8. The maximum instantaneous current the processor will draw while the thermal control circuit (TCC) is active as indicated by the assertion of PROCHOT# is the same as the maximum I_{CC} for the processor.
9. The core and cache portions of Stop-Grant current is specified at V_{CC} and V_{CACHE} max.
10. I_{CC_MAX} is specified at the relative V_{CC_MAX} point on the V_{CC} load line.

11. These parameters are based on design characterization and are not tested.
12. V_{TT} must be provided via a separate voltage source and must not be connected to V_{CC}.
13. These specifications are measured at the package pin.
14. Baseboard bandwidth is limited to 20 MHz.
15. This specification refers to a single processor with R_{TT} enabled.
16. This specification refers to a single processor with R_{TT} disabled.
17. The voltage specification requirements are measured across the $V_{CC\_CACHE\_SENSE}$ and $V_{SS\_CACHE\_SENSE}$ pins at the socket with a 100 MHz bandwidth oscilloscope, 1.5 pF maximum probe capacitance, and 1 MΩ minimum impedance. The maximum length of ground wire on the probe should be less than 5 mm. Ensure external noise from the system is not coupled into the scope probe.
18. This specification represents the V_{CC} reduction due to each VID transition. See Section 2.2.
19. This specification refers to the total reduction of the load line due to VID transitions below the specified VID.
20. I_{CC_TDC} is the sustained (DC equivalent) current that the processor is capable of drawing indefinitely and should be used for the voltage regulator temperature assessment. The voltage regulator is responsible for monitoring its temperature and asserting the necessary signal to inform the processor of a thermal excursion. The processor is capable of drawing I_{CC_TDC} indefinitely. Refer to Figure 2-3 for further details on the average processor current draw over various time durations. This parameter is based on design characterization and is not tested.
21. I_{TT} may draw up to 5A prior to power good assertion.

Figure 2-3. Processor Load Current vs. Time



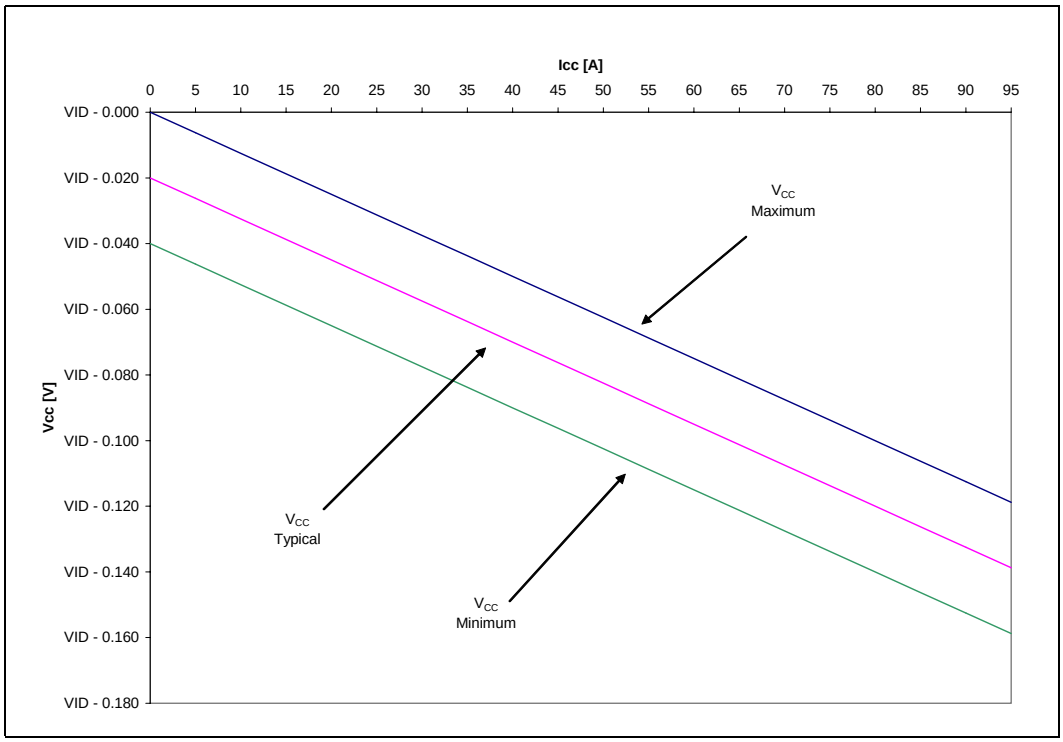
NOTES:
1. Processor or voltage regulator thermal protection circuitry should not trip for load currents greater than I_{CC_TDC}.
2. Not 100% tested. Specified by design characterization.

Table 2-10. V_{CC} Static and Transient Tolerance

$I_{CC\ [A]}$	V_{CC_MAX} [V]	V_{CC_TYP} [V]	V_{CC_MIN} [V]	Notes
0	VID - 0.000	VID - 0.020	VID - 0.040	1,2,3
5	VID - 0.006	VID - 0.026	VID - 0.046	1,2,3
10	VID - 0.013	VID - 0.033	VID - 0.053	1,2,3
15	VID - 0.019	VID - 0.039	VID - 0.059	1,2,3
20	VID - 0.025	VID - 0.045	VID - 0.065	1,2,3
25	VID - 0.031	VID - 0.051	VID - 0.071	1,2,3
30	VID - 0.038	VID - 0.058	VID - 0.078	1,2,3
35	VID - 0.044	VID - 0.064	VID - 0.084	1,2,3
40	VID - 0.050	VID - 0.070	VID - 0.090	1,2,3
45	VID - 0.056	VID - 0.076	VID - 0.096	1,2,3
50	VID - 0.063	VID - 0.083	VID - 0.103	1,2,3
55	VID - 0.069	VID - 0.089	VID - 0.109	1,2,3
60	VID - 0.075	VID - 0.095	VID - 0.115	1,2,3
65	VID - 0.081	VID - 0.101	VID - 0.121	1,2,3
70	VID - 0.087	VID - 0.108	VID - 0.128	1,2,3
75	VID - 0.094	VID - 0.114	VID - 0.134	1,2,3
80	VID - 0.100	VID - 0.120	VID - 0.140	1,2,3
85	VID - 0.106	VID - 0.126	VID - 0.146	1,2,3
90	VID - 0.113	VID - 0.133	VID - 0.153	1,2,3
95	VID - 0.119	VID - 0.139	VID - 0.159	1,2,3
100	VID - 0.125	VID - 0.145	VID - 0.165	1,2,3

NOTES:
1. The V_{CC_MIN} and V_{CC_MAX} load lines represent static and transient limits.
2. This table is intended to aid in reading discrete points on Figure 2-4.
3. The load lines specify voltage limits at the die measured at the $V_{CCSENSE}$ and $V_{SSSENSE}$ pins. Voltage regulation feedback for voltage regulator circuits must be taken from processor V_{CC} and V_{SS} pins.

Figure 2-4. V_{CC} Static and Transient Tolerance



NOTES:
1. The V_{CC_MIN} and V_{CC_MAX} load lines represent static and transient limits.
2. Refer to Table 2-9 for processor VID information for V_{CC}.
3. The load lines specify voltage limits at the die measured at the $V_{CCSENSE}$ and $V_{SSSENSE}$ pins. Voltage regulation feedback for voltage regulator circuits must also be taken from processor $V_{CCSENSE}$ and $V_{SSSENSE}$ pins.

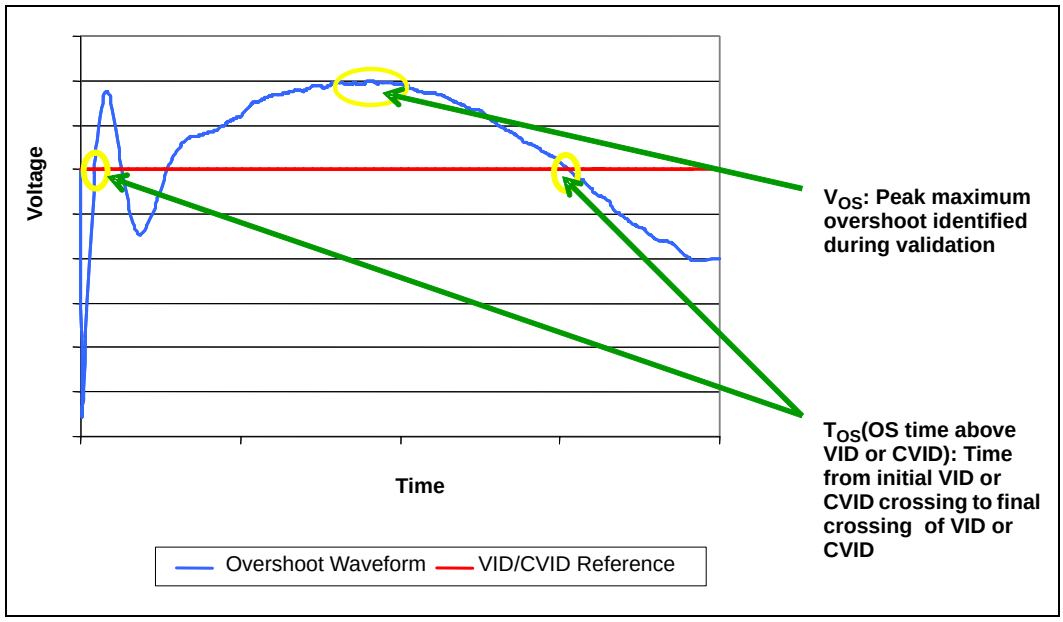
2.10.2 V_{CC} and V_{CACHE} Overshoot Specification

The processor can tolerate short transient overshoot events where V_{CC} exceeds the VID voltage or where V_{CACHE} exceeds the CVID voltage when transitioning from a high-to-low current load condition. This overshoot cannot exceed VID + V_{OS_MAX}, or CVID + V_{OS_MAX}. (V_{OS_MAX} is the maximum allowable overshoot above VID or CVID). These specifications apply to the processor die voltage as measured across the $V_{CCSENSE}$ and $V_{SSSENSE}$ pins for Vcc, and $V_{CC\_CACHE\_SENSE}$ and $V_{SS\_CACHE\_SENSE}$ pins for CVID.

Table 2-11. V_{CC} and V_{CACHE} Overshoot Specification

Symbol	Parameter	Min	Max	Units	Figure	Notes
V_{OS_MAX}	Magnitude of V_{CC} overshoot above VID or V_{CACHE} overshoot above CVID		0.025	V	2-5	
T_{OS_MAX}	Time duration of V_{CC} overshoot above VID or V_{CACHE} overshoot above CVID		5	µs	2-5	

Figure 2-5. V_{CC} and V_{CACHE} Overshoot Example Waveform



2.10.3 Die Voltage Validation

Overshoot events from application testing on the processor must meet the specifications in Table 2-11 when measured across the $V_{CCSENSE}$ and $V_{SSSENSE}$ pins. Overshoot events that are < 10 ns in duration may be ignored. These measurements of processor die level overshoot should be taken with a 100 MHz bandwidth limited oscilloscope.

Table 2-12. Front Side Bus Differential BCLK Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Figure	Notes
V_L	Input Low Voltage	-0.150	0.000	N/A	V	2-8	
V_H	Input High Voltage	0.660	0.700	0.850	V	2-8	
$V_{CROSS(abs)}$	Absolute Crossing Point	0.250	N/A	0.550	V	2-8, 2-9	1,7
$V_{CROSS(rel)}$	Relative Crossing Point	0.250 + 0.5* (V_{Havg} - 0.700)	N/A	0.550 + 0.5* (V_{Havg} - 0.700)	V	2-8, 2-9	2,7,8
ΔV_{CROSS}	Range of Crossing Point	N/A	N/A	0.140	V	2-8, 2-9	
V_{OV}	Overshoot	N/A	N/A	+ 0.300	V	2-8	3
V_{US}	Undershoot	- 0.300	N/A	N/A	V	2-8	4
V_{RBM}	Ringback Margin	0.200	N/A	N/A	V	2-8	5
V_{TM}	Threshold Margin	V_{CROSS}-0.100		V_{CROSS}+0.100	V	2-8	6

NOTES:
1. Crossing voltage is defined as the instantaneous voltage value when the rising edge of BCLK0 is equal to the falling edge of BCLK1.
2. V_{Havg} is the statistical average of the V_H measured by the oscilloscope.
3. Overshoot is defined as the absolute value of the maximum voltage.

4. Undershoot is defined as the absolute value of the minimum voltage.
5. Ringback Margin is defined as the absolute voltage difference between the maximum Rising Edge Ringback and the maximum Falling Edge Ringback.
6. Threshold Region is defined as a region entered around the crossing point voltage in which the differential receiver switches. It includes input threshold hysteresis.
7. The crossing point must meet the absolute and relative crossing point specifications simultaneously.
8. V_{Havg} can be measured directly using “Vtop” on Agilent scopes and “High” on Tektronix scopes.

Table 2-13. BSEL[1:0], VID[5:0], and CVID[3:0] DC Specifications

Symbol	Parameter	Max	Unit	Notes
R_{ON}	Buffer On Resistance	60	Ω	1
I_{OL}	Max Pin Current	8	mA	
I_{LO}	Output Leakage Current	200	µA	2
V_{TOL}	Voltage Tolerance	3.3 * 1.05	V	3

NOTES:
1. These parameters are not tested and are based on design simulations.
2. Leakage to V_{SS} with pin held at 2.5V.
3. Represents the maximum allowable termination voltage.

Table 2-14. VIDPWRGD DC Specifications

Symbol	Parameter	Min	Max	Unit	Figure	Notes
V_{IL}	Input Low Voltage	0.0	0.30	V	2-19	
V_{IH}	Input High Voltage	0.90	V_{TT}	V	2-19	

Table 2-15. AGTL+ Signal Group DC Specifications

Symbol	Parameter	Min	Max	Unit	Notes
V_{IL}	Input Low Voltage	0.0	GTLREF - (0.10 * V_{TT})	V	1,5
V_{IH}	Input High Voltage	GTLREF + (0.10 * V_{TT})	V_{TT}	V	2,3,5
V_{OH}	Output High Voltage	0.90 * V_{TT}	V_{TT}	V	3,5
I_{OL}	Output Low Current	N/A	V_{TT} / (0.50 * Rtt_min + R_{ON}_min || R_L)	mA	7
I_{LI}	Input Leakage Current	N/A	± 200	µA	6
I_{LO}	Output Leakage Current	N/A	± 200	µA	8
R_{ON}	Buffer On Resistance	8	12	W	4

NOTES:
1. V_{IL} is defined as the voltage level at a receiving agent that will be interpreted as a logical low value.
2. V_{IH} is defined as the voltage level at a receiving agent that will be interpreted as a logical high value.
3. V_{IH} and V_{OH} may experience excursions above V_{CC}. However, input signal drivers must comply with the signal quality specifications in Section 3.
4. Refer to Processor Signal Integrity Models for I/V characteristics.
5. The V_{TT} referred to in these specifications refers to the instantaneous V_{TT}.
6. Leakage to V_{SS} with pin held at V_{TT}.
7. The maximum output current is based on maximum current handling capability of the buffer and is not specified into the test load.
8. Leakage to V_{TT} with pin held at 300 mV.

Table 2-16. PWRGOOD and TAP Signal Group DC Specifications

Symbol	Parameter	Min	Max	Unit	Notes[1]
V_{HYS}	Input Hysteresis	200	350	mV	6
V_{T+}	Input Low to High Threshold Voltage	0.5 * (V_{TT} + V_{HYS_MIN})	0.5 * (V_{TT} + V_{HYS_MAX})	V	4
V_{T-}	Input High to Low Threshold Voltage	0.5 * (V_{TT} - V_{HYS_MAX})	0.5 * (V_{TT} - V_{HYS_MIN})	V	4
V_{OH}	Output High Voltage	N/A	V_{TT}	V	2,4
I_{OL}	Output Low Current		45	mA	5
I_{LI}	Input Leakage Current		±200	µA	
I_{LO}	Output Leakage Current		±200	µA	
R_{ON}	Buffer On Resistance	8	12	Ω	3

NOTES:
1. All outputs are open drain.
2. TAP signal group must meet system signal quality specification in Section 3.
3. Refer to the Processor Signal Integrity Models for I/V characteristics.
4. The V_{TT} referred to in these specifications refers to instantaneous V_{TT}.
5. The maximum output current is based on maximum current handling capability of the buffer and is not specified into the test load.
6. V_{HYS} represents the amount of hysteresis, nominally centered about 0.5 * V_{TT} for all TAP inputs.

Table 2-17. GTL+ and AGTL+ Asynchronous Signal Group DC Specifications

Symbol	Parameter	Min	Max	Unit	Notes
V_{IL}	Input Low Voltage	0	GTLREF - (10% * V_{TT})	V	2
V_{IH}	Input High Voltage	GTLREF + (10% * V_{TT})	V_{TT}	V	3,4,6
V_{OH}	Output High Voltage		V_{TT}	V	1,4,6
I_{OL}	Output Low Current		50	mA	7
I_{LI}	Input Leakage Current	N/A	± 200	µA	8
I_{LO}	Output Leakage Current		± 200	µA	9
R_{on}	Buffer On Resistance	8	12	Ω	5

NOTES:
1. All outputs are open-drain.
2. V_{IL} is defined as the voltage range at a receiving agent that will be interpreted as a logical low value.
3. V_{IH} is defined as the voltage range at a receiving agent that will be interpreted as a logical high value.
4. V_{IH} and V_{OH} may experience excursions above V_{TT}. However, input signal drivers must comply with the signal quality specifications in Section 3.
5. Refer to the Processor Signal Integrity Models for I/V characteristics.
6. The V_{TT} referred to in these specifications refers to instantaneous V_{TT}.
7. The maximum output current is based on maximum current handling capability of the buffer and is not specified into the test load.
8. Leakage to V_{SS} with pin held at V_{TT}
9. Leakage to V_{TT} with pin held at 300 mV.

Table 2-18. SMBus Signal Group DC Specifications

Symbol	Parameter	Min	Max	Unit	Notes [1,2]
V_{IL}	Input Low Voltage	-0.30	0.30 * SM_VCC	V	
V_{IH}	Input High Voltage	0.70 * SM_VCC	3.465	V	
V_{OL}	Output Low Voltage	0	0.400	V	
I_{OL}	Output Low Current	N/A	3.0	mA	
I_{LI}	Input Leakage Current	N/A	± 10	µA	
I_{LO}	Output Leakage Current	N/A	± 10	µA	
C_{SMB}	SMBus Pin Capacitance		15.0	pF	3

NOTES:
1. These parameters are based on design characterization and are not tested.
2. All DC specifications for the SMBus signal group are measured at the processor pins.
3. Platform designers may need this value to calculate the maximum loading of the SMBus and to determine maximum rise and fall times for SMBus signals.

2.11 AGTL+ Front Side Bus Specifications

Termination resistors are not required for most AGTL+ signals because they are integrated into the processor silicon.

Valid high and low levels are determined by the input buffers which compare a signal's voltage with a reference voltage called GTLREF.

Table 2-19 lists the GTLREF specifications. GTLREF should be generated on the system board using high-precision voltage divider circuits.

Table 2-19. AGTL+ Bus Voltage Definitions

Symbol	Parameter	Min	Typ	Max	Units	Notes
GTLREF	Bus Reference Voltage	0.98 * (0.63 * V_{TT})	0.63 * V_{TT}	1.02 * (0.63 * V_{TT})	V	1,2,6
R_{TT}	Termination Resistance (pull-up)	40.5	45	49.5	Ω	3
R_L	Termination Resistance (pull-down)	360	450	540	Ω	4
COMP0	COMP Resistance	49.4	49.9	50.4	Ω	5
SLEW_CTRL	SLEW_CTRL Resistance	49.4	49.9	50.4	Ω	7

NOTES:
1. The tolerances for this specification have been stated generically to enable system designers to calculate the minimum values across the range of V_{TT}.
2. GTLREF is generated from V_{TT} on the baseboard by a voltage divider of 1% resistors.
3. R_{TT} is the on-die termination resistance measured at V_{OL} of the AGTL+ output driver.
4. R_L is the on-die termination resistance for improved noise margin and signal integrity.
5. The COMP0 resistor is provided by the baseboard with 1% resistors.
6. The V_{TT} referred to in these specifications refers to instantaneous V_{TT}.
7. The SLEW_CTRL resistor is provided by the baseboard with 1% resistors.

2.12 Front Side Bus AC Specifications

The processor front side bus timings specified in this section are defined at the processor core silicon and are thus not measurable at the processor pins.

See Section 6 for processor pin signal definitions.

Table 2-20 through Table 2-27 list the AC specifications associated with the processor front side bus.

All AGTL+ timings are referenced to GTLREF for both '0' and '1' logic levels unless otherwise specified.

Table 2-20. Front Side Bus Differential Clock Specifications

T# Parameter	Min	Nom	Max	Unit	Figure	Notes[1]
FSB Clock Frequency	165.78		166.72	MHz		
T1: BCLK[1:0] Period	5.9982		6.0320	ns	2-8	2
T2: BCLK[1:0] Period Stability			175	ps		3,4
T3: BCLK[1:0] Rise Time	175		700	ps		5
T4: BCLK[1:0] Fall Time	175		700	ps		5

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor core frequencies based on a 166 MHz BCLK[1:0].
2. The period specified here is the average period. A given period may vary from this specification as governed by the period stability specification (T2). Min period specification is based on -300 PPM deviation from a 6 ns period. Max period specification is based on the summation of +300 PPM deviation from a 6 ns period and a +0.5% maximum variance due to spread spectrum clocking.
3. For the clock jitter specification, refer to the applicable clock driver design specification.
4. In this context, period stability is defined as the worst case timing difference between successive crossover voltages. In other words, the largest absolute difference between adjacent clock periods must be less than the period stability.
5. Rise and fall times are measured single-ended between 245 mV and 455 mV of the clock swing.

Table 2-21. Front Side Bus Common Clock AC Specifications

T# Parameter	Min	Max	Unit	Figure	Notes [1, 2]
T10: Common Clock Output Valid Delay	-0.125	1.470	ns	2-10	3
T11: Common Clock Input Setup Time	0.810	N/A	ns	2-10	4
T12: Common Clock Input Hold Time	0.355	N/A	ns	2-10	4
T13: RESET# Pulse Width	1.00	10.00	ms	2-18	5,6,7

NOTES:
1. These parameters are based on design characterization and are not tested.
2. All common clock AC timings for AGTL+ signals are referenced to the Crossing Voltage (V_{CROSS}) of the BCLK[1:0] at rising edge of BCLK0. All common clock AGTL+ signal timings are referenced at GTLREF at the processor core.
3. Valid delay timings for these signals are specified into the test circuit described in Figure 2-6 and with GTLREF at 0.63 * V_{TT} ± 2%.
4. Specification is for a minimum swing defined between V_{IL_MAX} to V_{IH_MIN}. This assumes an edge rate of 0.9 V/ns to 1.2 V/ns.
5. RESET# can be asserted (active) asynchronously, but must be deasserted synchronously.
6. This should be measured after V_{TT} and BCLK[1:0] become stable.
7. Maximum specification applies only while PWRGOOD is asserted.

Table 2-22. Front Side Bus Source Synchronous AC Specifications (Sheet 1 of 2)

T# Parameter	Min	Typ	Max	Unit	Figure	Notes 1,2,3
T20: Source Sync. Output Valid Delay (first data/address only)	-0.150		1.400	ns	2-11,2-12	4
T21: T_{VBD} Source Sync. Data Output Valid Before Data Strobe	0.400			ns	2-12	4,7
T22: T_{VAD} Source Sync. Data Output Valid After Data Strobe	0.400			ns	2-12	4,8

Table 2-22. Front Side Bus Source Synchronous AC Specifications (Sheet 2 of 2)

T# Parameter	Min	Typ	Max	Unit	Figure	Notes 1,2,3
T23: T_{VBA} Source Sync. Address Output Valid Before Address Strobe	1.120			ns	2-11	4,7
T24: T_{VAA} Source Sync. Address Output Valid After Address Strobe	1.120			ns	2-11	4,8
T25: T_{SUSS} Source Sync. Input Setup Time to Strobe	0.100			ns	2-11,2-12	5
T26: T_{HSS} Source Sync. Input Hold Time to Strobe	0.100			ns	2-11,2-12	5
T27: T_{SUCC} Source Sync. Input Setup Time to BCLK[1:0]	0.910			ns	2-11,2-12	6
T29: T_{FASS} First Address Strobe to Second Address Strobe		1/2		BCLKs	2-11	9
T30: T_{FDSS}: First Data Strobe to Subsequent Strobes		n/4		BCLKs	2-12	10,11
T31: Data Strobe ‘n’ (DSTBN#) Output Valid Delay	5.100		6.650	ns	2-12	12
T32: Address Strobe Output Valid Delay	1.350		2.900	ns	2-11	

NOTES:
1. Not 100% tested. These parameters are based on design characterization.
2. All source synchronous AC timings are referenced to their associated strobe at GTLREF. Source synchronous data signals are referenced to the falling edge of their associated data strobe. Source synchronous address signals are referenced to the rising and falling edge of their associated address strobe. All source synchronous AGTL+ signal timings are referenced at GTLREF at the processor core.
3. Unless otherwise noted, these specifications apply to both data and address timings.
4. Valid delay timings for these signals are specified into the test circuit described in Figure 2-6 and with GTLREF at 0.63 * V_{TT} ± 2%.
5. Specification is for a minimum swing defined between V_{IL_MAX} to V_{IH_MIN}. AC timings are specified as GTLREF ± (0.06 * V_{TT}). This assumes an edge rate of 0.9 V/ns to 1.2 V/ns.
6. All source synchronous signals must meet the specified setup time to BCLK as well as the setup time to each respective strobe.
7. This specification represents the minimum time the data or address will be valid before its strobe.
8. This specification represents the minimum time the data or address will be valid after its strobe.
9. The rising edge of ADSTB# must come approximately 1/2 BCLK period after the falling edge of ADSTB#.
10. For this timing parameter, n = 1, 2, and 3 for the second, third, and last data strobes respectively.
11. The second data strobe (falling edge of DSTBn#) must come approximately 1/4 BCLK period after the first falling edge of DSTBp#. The third data strobe (falling edge of DSTBp#) must come approximately 1/2 BCLK period after the first falling edge of DSTBp#. The last data strobe (falling edge of DSTBn#) must come approximately 3/4 BCLK period after the first falling edge of DSTBp#.
12. This specification applies only to DSTBN[3:0]# and is measured to the second falling edge of the strobe.

Table 2-23. Miscellaneous Signals AC Specifications (Sheet 1 of 2)

T# Parameter	Min	Max	Unit	Figure	Notes 1,2,5
T35: GTL+ asynchronous and AGTL+ asynchronous input pulse width	6		BCLKs		7
T36: PWRGOOD to RESET# deassertion time	1	10	ms	2-18	
T37: BCLK valid before PWRGOOD active	10		BCLKs	2-18	3

Table 2-23. Miscellaneous Signals AC Specifications (Sheet 2 of 2)

T# Parameter	Min	Max	Unit	Figure	Notes 1,2,5
T38: PROCHOT#, FORCEPR# pulse width	500		µs	2-14	4
T39: THERMTRIP# assertion until V_{CC} and V_{CACHE} removal		500	ms	2-15	6
T40: FERR# valid delay from STPCLK# deassertion	0	5	BCLKs	2-20	
T41: V_{CC} to PWRGOOD assertion time	1	500	ms	2-18	

NOTES:
1. All AC timings for the GTL+ asynchronous signals are referenced to the BCLK0 rising edge at Crossing Voltage (V_{CROSS}). All GTL+ asynchronous signal timings are referenced at GTLREF. PWRGOOD is referenced to the BCLK0 rising edge at 0.5 * V_{TT}.
2. These signals may be driven asynchronously.
3. Refer to the PWRGOOD definition for more details regarding the behavior of the signal.
4. Length of assertion for PROCHOT# does not equal TCC activation time. Time is required after the assertion or deassertion of PROCHOT# for the processor to enable or disable the TCC. Additionally, time is allocated after the assertion or deassertion of PROCHOT# for the processor to complete current instruction execution. This specification applies to the PROCHOT# signal when asserted by the processor and the FORCEPR# signal when asserted by the system.
5. Refer to Section 8.2 for additional timing requirements for entering and leaving low power states.
6. Intel recommends the V_{TT} power supply also be removed upon assertion of THERMTRIP#.
7. A minimum pulse width of 500us is recommended when FORCEPR# is asserted by the system.

Table 2-24. Front Side Bus AC Specifications (Reset Conditions)

T# Parameter	Min	Max	Unit	Figure	Notes
T47: Reset Configuration Signals (A[21:16]#) Setup Time	1		ms		1
T45: Reset Configuration Signals (A[39:22]#, A[15:3]#, BR[3:0]#, INIT#, SMI#) Setup Time	4		BCLKs	2-18	1
T46: Reset Configuration Signals (A[39:3]#, BR[3:0]#, INIT#, SMI#) Hold Time	2	28	BCLKs	2-18	2

NOTES:
1. Before the clock that de-asserts RESET#
2. After the clock that de-asserts RESET#.

Table 2-25. TAP Signal Group AC Specifications

T# Parameter	Min	Max	Unit	Figure	Notes 1,7
T55: TCK Period	13.3		ns	2-7	2
T61: TDI, TMS Setup Time	1.5		ns	2-13	3,6
T62: TDI, TMS Hold Time	3.0		ns	2-13	3,6
T63: TDO Clock to Output Delay	0.5	10.0	ns	2-13	4
T64: TRST# Assert Time	2		TCK	2-14	5

NOTES:
1. Not 100% tested. These parameters are based on design characterization.
2. This specification is based on the capabilities of the ITP-XDP debug port tool, not on processor silicon.
3. Referenced to the rising edge of TCK.
4. Referenced to the falling edge of TCK.
5. TRST# must be held asserted for 2 TCK periods to be guaranteed that it is recognized by the processor.

6. Specification for a minimum swing defined between TAP V_{T-} to V_{T+}. This assumes a minimum edge rate of 0.5 V/ns.
7. It is recommended that TMS be asserted while TRST# is being deasserted.

Table 2-26. VIDPWRGD and Other Voltage Sequence AC Specifications

T# Parameter	Min	Max	Unit	Figure	Notes
T70: VIDPWRGD rise time		150	ns	2-19	1
T71: V_{TT} to VIDPWRGD delay time	1	10	ms	2-19	
T72: V_{TT} to VIDPWRGD deassertion time		1	ms	2-19	2
T73: VIDPWRGD to V_{CACHE} delay time	0		ms	2-18	
T74: V_{CACHE} to V_{CC} delay time	1		ms	2-18	3

NOTES:
1. Rise time is measured between 10% and 90% points on the waveform.
2. Specification refers to the time between VIDPWRGD = V_{TT} - 20% and VIDPWRGD = V_{IL}.
3. V_{CACHE} to V_{CC} delay time is measured from (0.5 * CVID) to (0.5 * VID).

Table 2-27. VID Signal Group AC Timing Specifications

T# Parameter	Min	Max	Unit	Figure	Notes
T80: VID Step Time	5		µs	2-21, 2-22	
T81: VID Dwell Time	50		µs	2-21, 2-22	
T82: VID Down Transition to Valid V_{CC} (min)		0	µs	2-21	
T82: VID Up Transition to Valid V_{CC} (min)		50	µs	2-21	
T82: VID Down Transition to Valid V_{CC} (max)		50	µs	2-22	
T82: VID Up Transition to Valid V_{CC} (max)		0	µs	2-22	

Table 2-28. SMBus Signal Group AC Specifications

T# Parameter	Min	Max	Unit	Figure	Notes [1,2]
T90: SM_CLK Frequency	10	100	KHz		
T91: SM_CLK Period	10	100	µs		
T92: SM_CLK High Time	4.0	N/A	µs	2-16	
T93: SM_CLK Low Time	4.7	N/A	µs	2-16	
T94: SMBus Rise Time	0.02	1.0	µs	2-16	4
T95: SMBus Fall Time	0.02	0.3	µs	2-16	4
T96: SMBus Output Valid Delay	0.1	4.5	µs	2-17	
T97: SMBus Input Setup Time	250	N/A	ns	2-16	
T98: SMBus Input Hold Time	300	N/A	ns	2-16	
T99: Bus Free Time	4.7	N/A	µs	2-16	3,5
T100: Hold Time after Repeated Start Condition	4.0	N/A	µs	2-16	
T101: Repeated Start Condition Setup Time	4.7	N/A	µs	2-16	
T102: Stop Condition Setup Time	4.0	N/A	µs	2-16	

NOTES:
1. These parameters are based on design characterization and are not tested.
2. All AC timings for the SMBus signals are referenced at V_{IL_MAX} or V_{IL_MIN} and measured at the processor pins. Refer to Figure 2-16.
3. Minimum time allowed between request cycles.
4. Rise time is measured from (V_{IL_MAX} - 0.15V) to (V_{IH_MIN} + 0.15V). Fall time is measured from (0.9 * SM_VCC) to (V_{IL_MAX} - 0.15V). DC parameters are specified in Table 2-18.
5. Following a write transaction, an internal write cycle time of 10ms must be allowed before starting the next transaction

2.13 Processor AC Timing Waveforms

The following figures are used in conjunction with the AC timing tables (Table 2-21 through Table 2-28).

Note: For Figure 2-7 through Figure 2-19, the following apply:

1. All common clock AC timings for AGTL+ signals are referenced to the Crossing Voltage (V_{CROSS}) of the BCLK[1:0] at rising edge of BCLK0. All common clock AGTL+ signal timings are referenced at GTLREF at the processor core.
2. All source synchronous AC timings for AGTL+ signals are referenced to their associated strobe (address or data) at GTLREF. Source synchronous data signals are referenced to the falling edge of their associated data strobe. Source synchronous address signals are referenced to the rising and falling edge of their associated address strobe. All source synchronous AGTL+ signal timings are referenced at GTLREF at the processor silicon.
3. All AC timings for AGTL+ strobe signals are referenced to BCLK[1:0] at V_{CROSS}. All AGTL+ strobe signal timings are referenced at GTLREF at the processor silicon.
4. All AC timings for the TAP signals are referenced to the TCK at 0.5 * V_{TT} at the processor pins. All TAP signal timings (TMS, TDI, etc.) are referenced at 0.5 * V_{TT} at the processor pins.
5. All AC timings for the SMBus signals are referenced to the SM_CLK at 0.5 * SM_VCC at the processor pins. All SMBus signal timings (SM_DAT, SM_CLK, etc.) are referenced at V_{IL_MAX} or V_{IL_MIN} at the processor pins.

Figure 2-6. Electrical Test Circuit

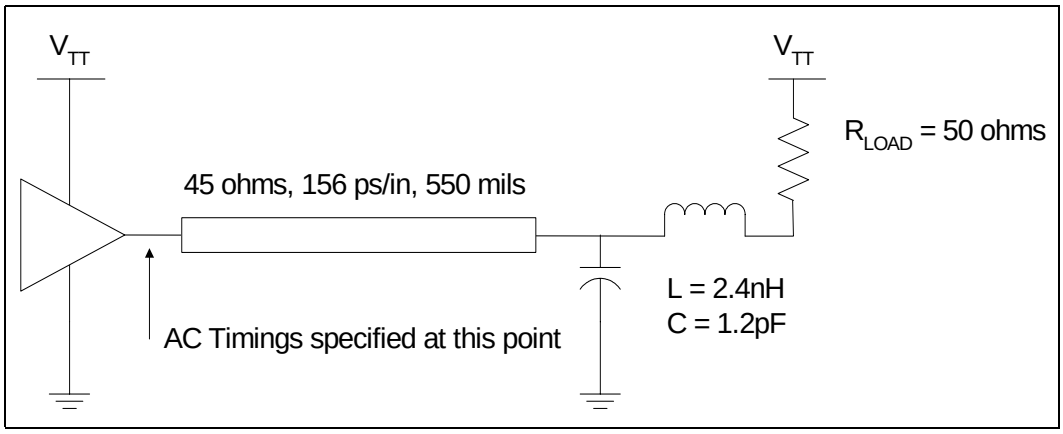


Figure 2-7. TCK Clock Waveform

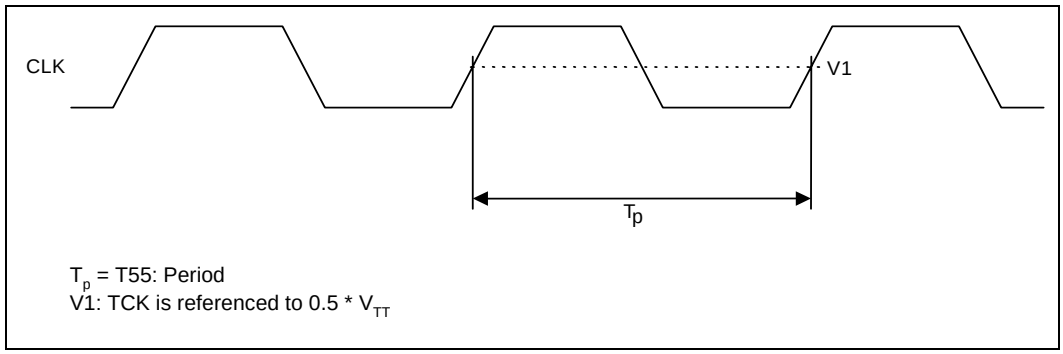


Figure 2-8. Differential Clock Waveform

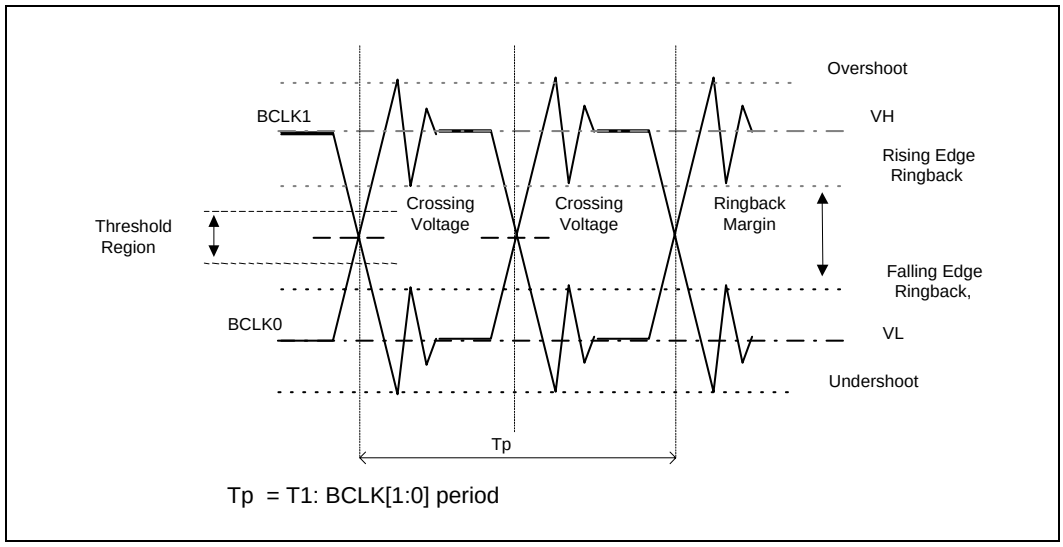


Figure 2-9. Differential Clock Crosspoint Specification

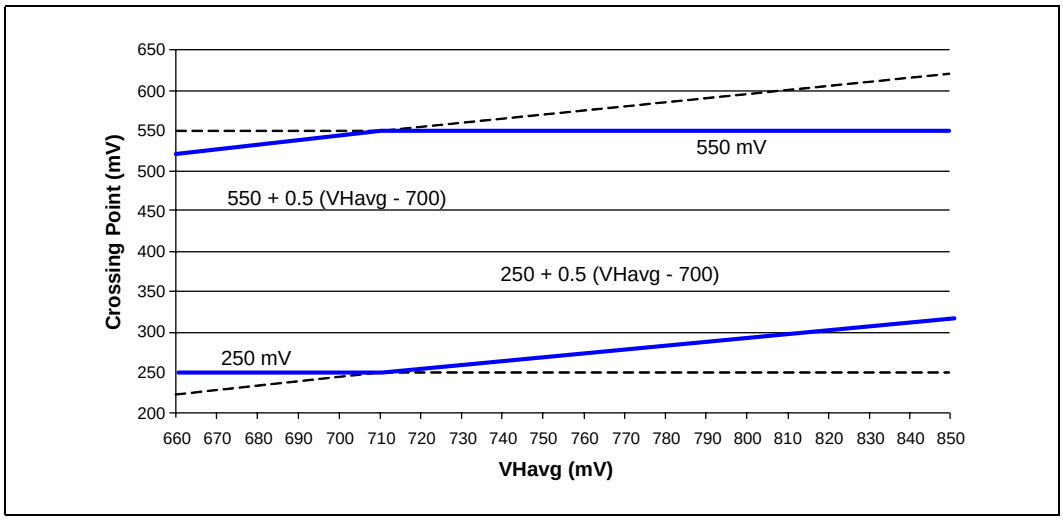


Figure 2-10. Front Side Bus Common Clock Valid Delay Timing Waveform

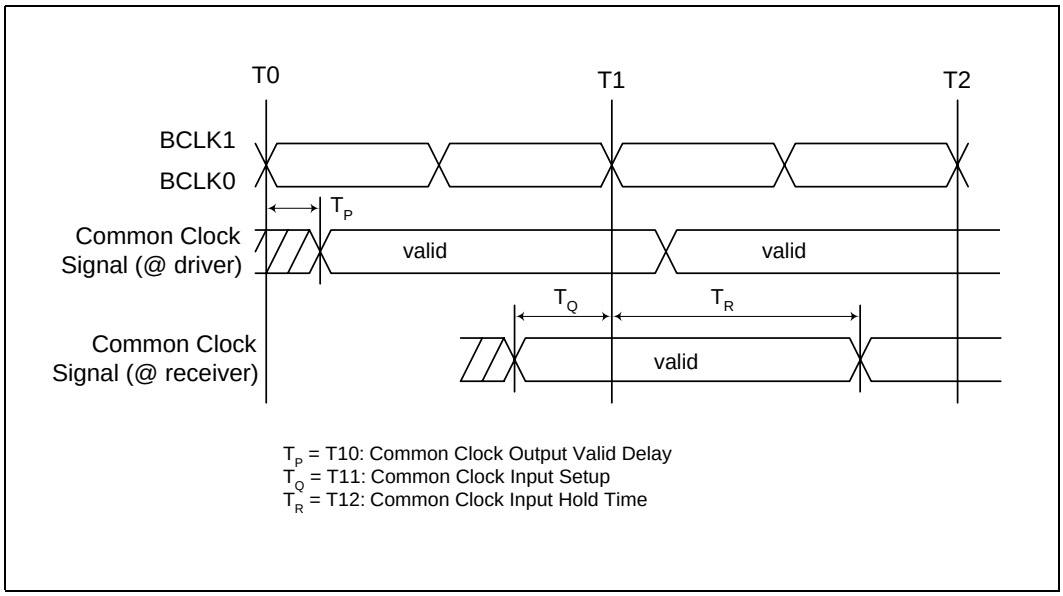


Figure 2-11. Source Synchronous 2X (Address) Timing Waveform

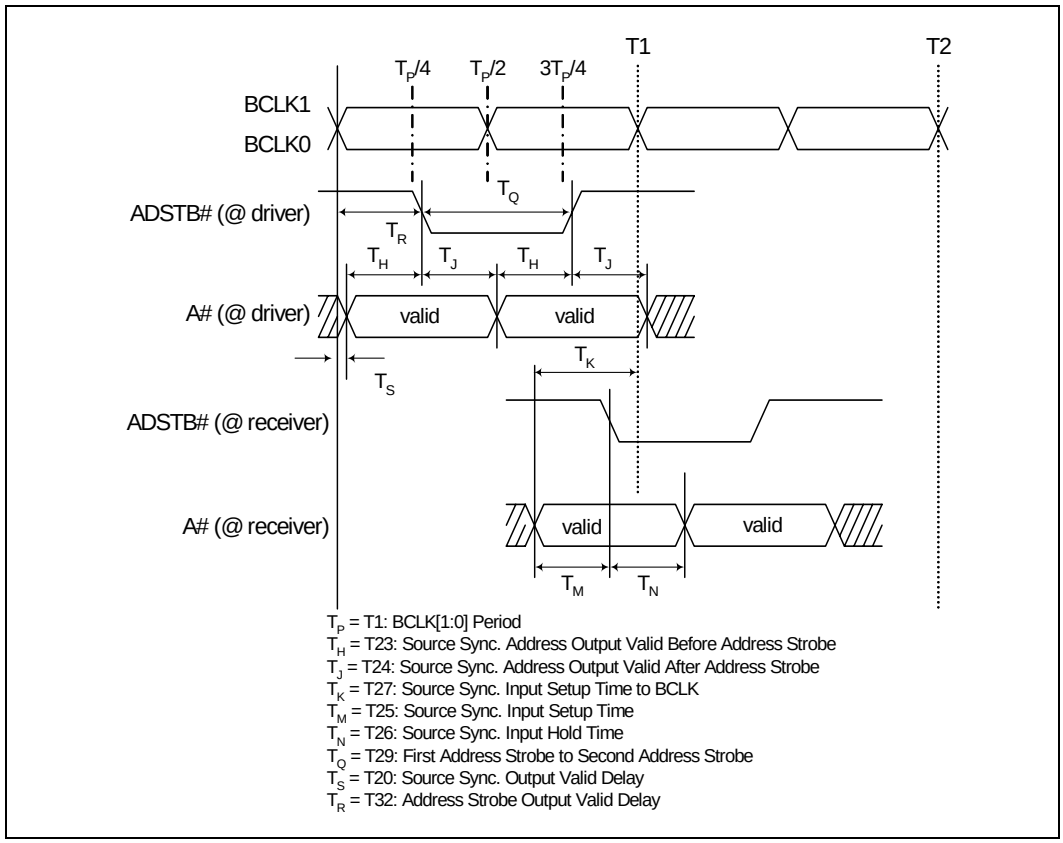
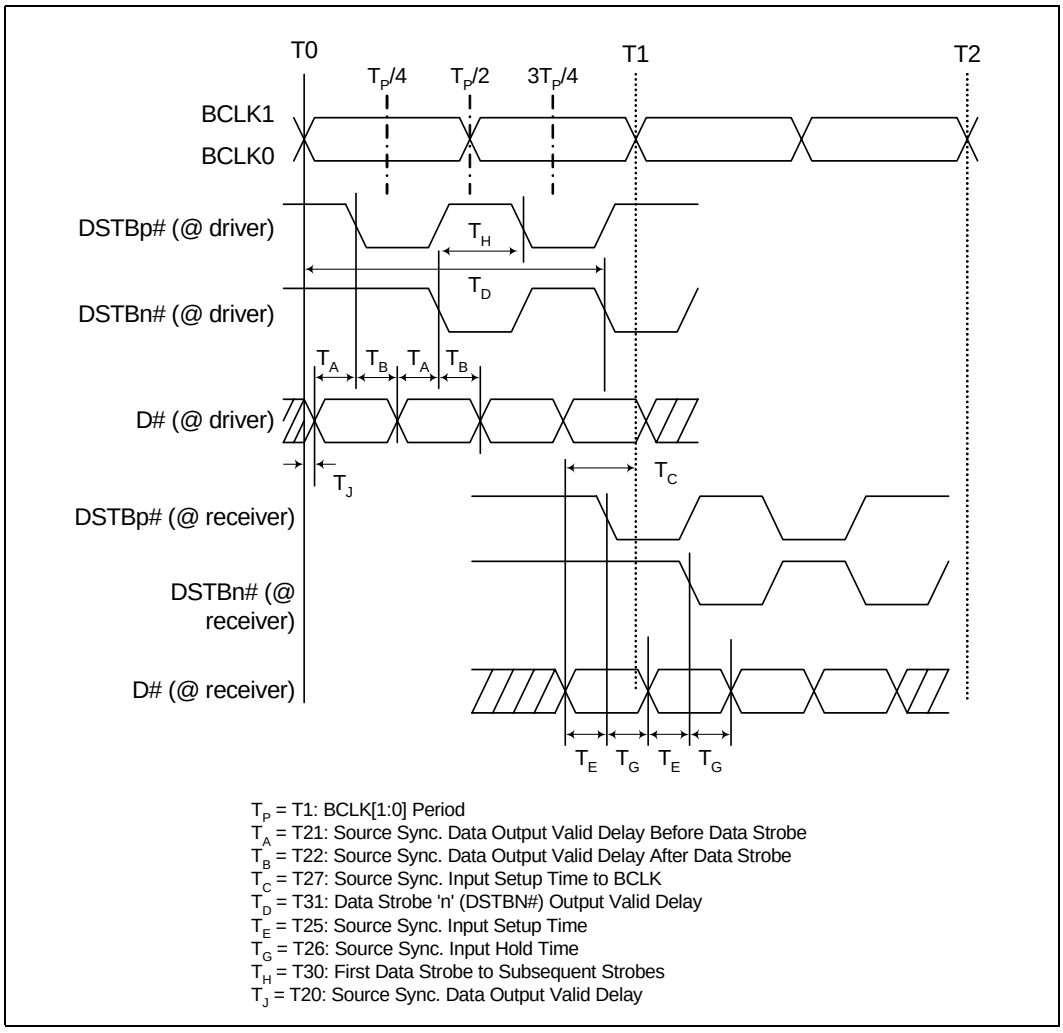


Figure 2-12. Source Synchronous 4X (Data) Timing Waveform



T_P = T1: BCLK[1:0] Period
T_A = T21: Source Sync. Data Output Valid Delay Before Data Strobe
T_B = T22: Source Sync. Data Output Valid Delay After Data Strobe
T_C = T27: Source Sync. Input Setup Time to BCLK
T_D = T31: Data Strobe 'n' (DSTBN#) Output Valid Delay
T_E = T25: Source Sync. Input Setup Time
T_G = T26: Source Sync. Input Hold Time
T_H = T30: First Data Strobe to Subsequent Strobes
T_J = T20: Source Sync. Data Output Valid Delay

Figure 2-13. TAP Valid Delay Timing Waveform

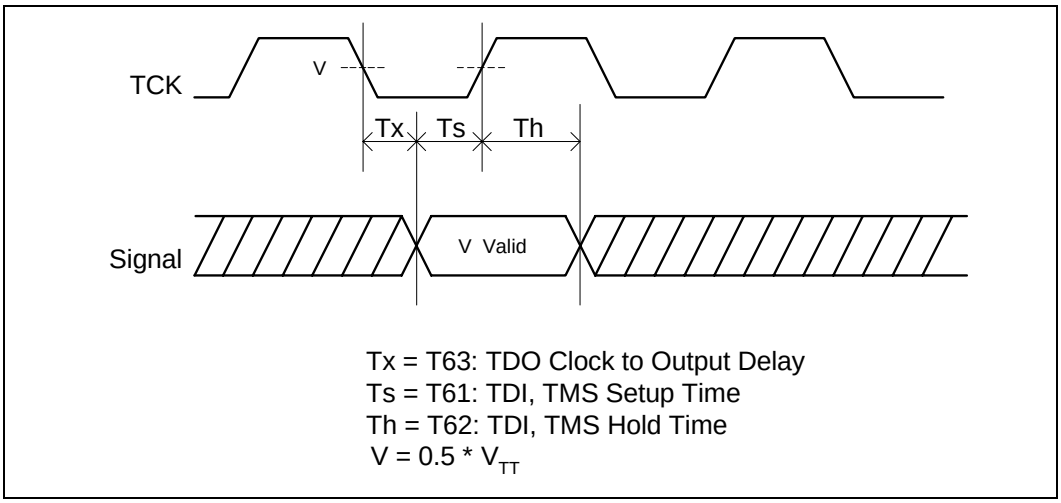


Figure 2-14. Test Reset (TRST#), Async GTL+ Input, and PROCHOT# Timing Waveform

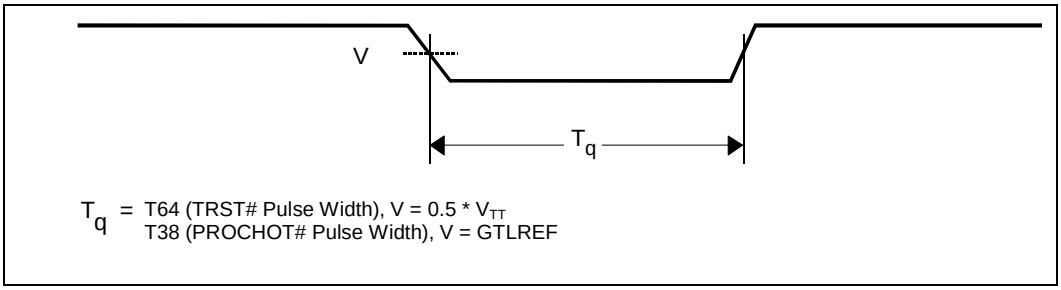


Figure 2-15. THERMTRIP# Power Down Sequence

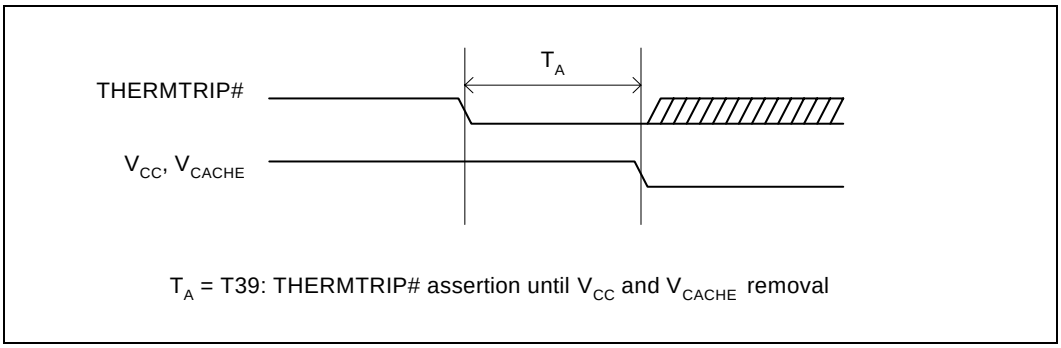


Figure 2-16. SMBus Timing Waveform

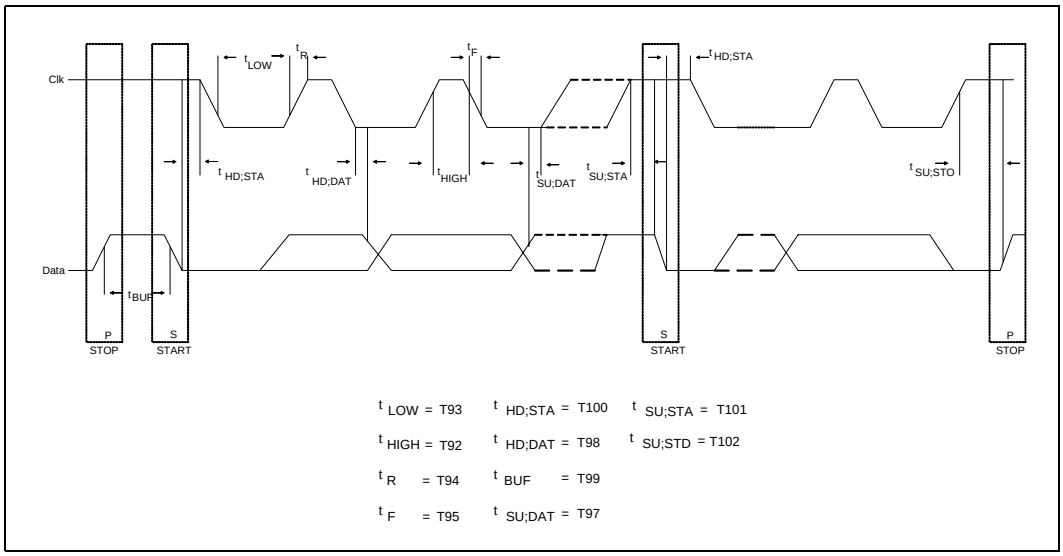


Figure 2-17. SMBus Valid Delay Timing Waveform

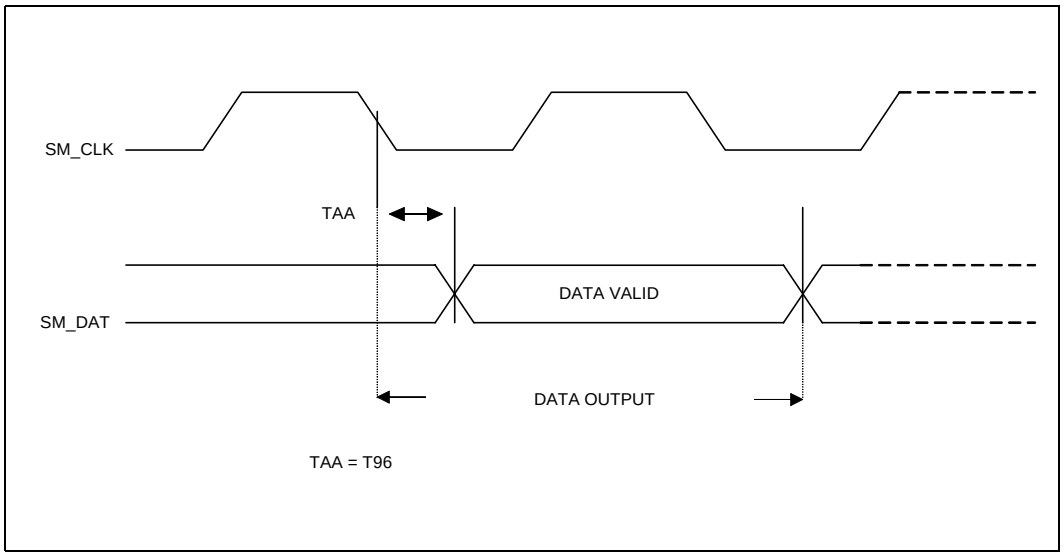


Figure 2-18. Voltage Sequence Timing Requirements

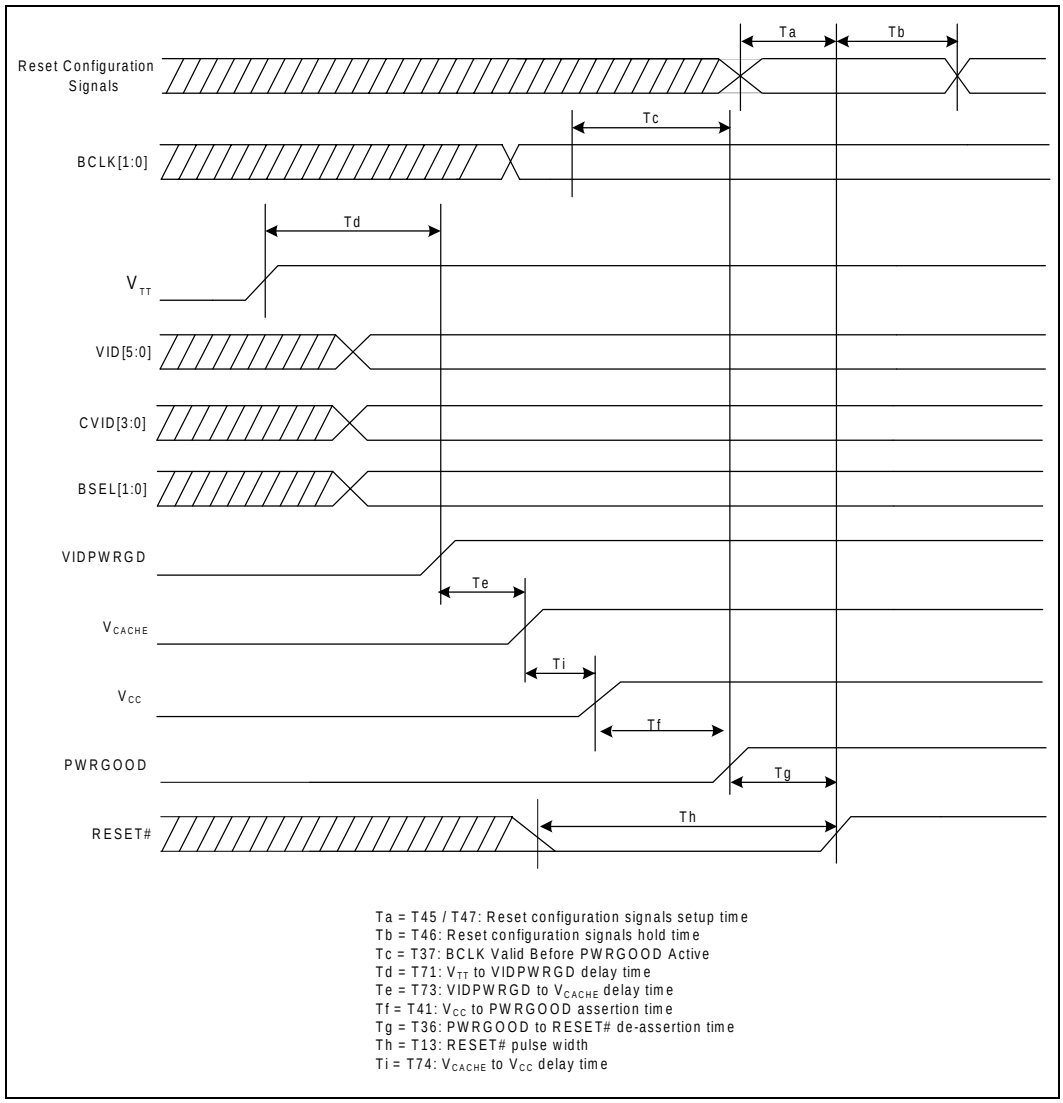
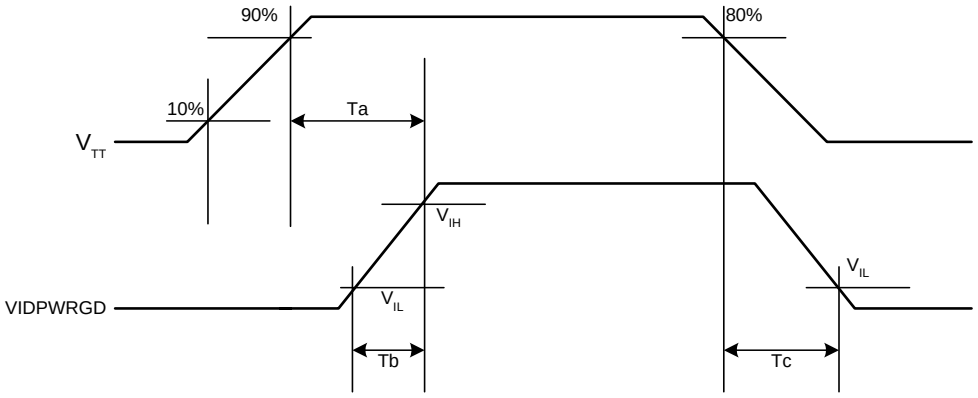
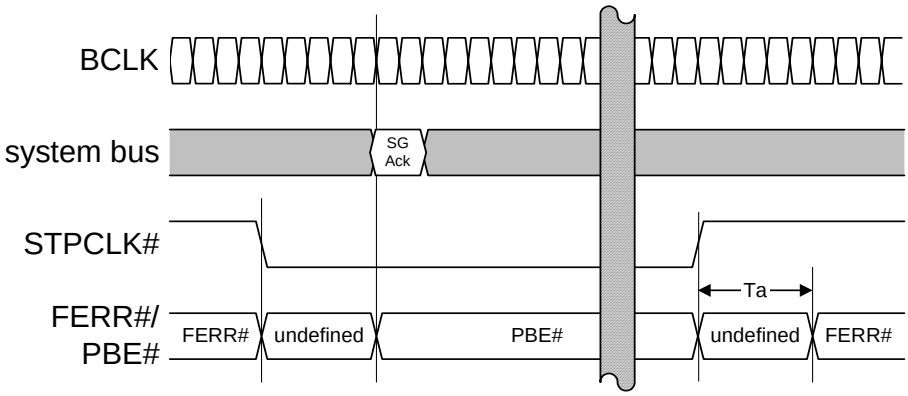


Figure 2-19. VIDPWRGD Timing Requirements



Ta = T71 V_{TT} to VIDPWRGD delay time
Tb = T70 VIDPWRGD rise time
Tc = T72 V_{TT} to VIDPWRGD deassertion time

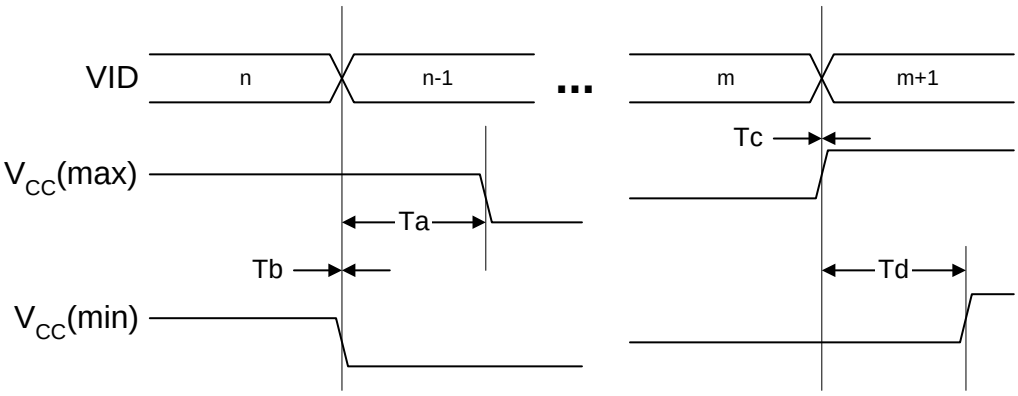
Figure 2-20. FERR#/PBE# Valid Delay Timing



Ta = T40: FERR# valid delay from STPCLK# de-assertion

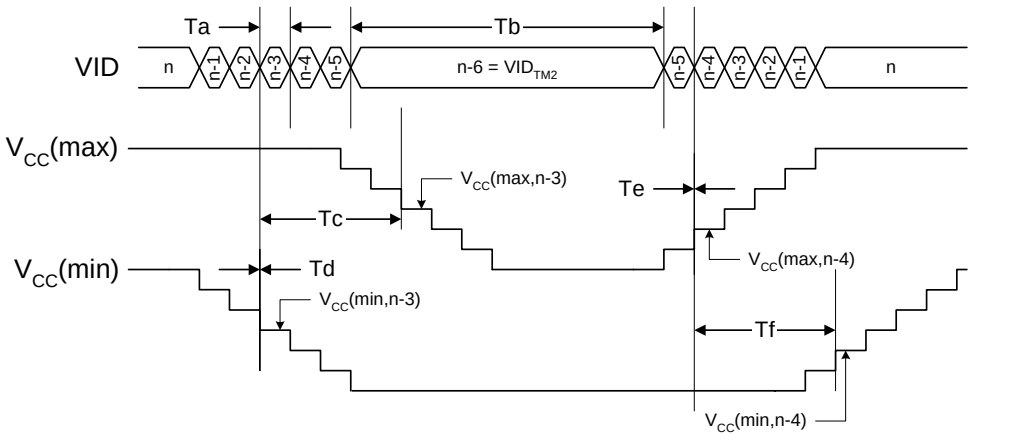
Note: FERR#/PBE# is also undefined from STPCLK# assertion until the stop grant acknowledge is driven on the processor system bus. FERR#/PBE# is also undefined for a period of Ta from STPCLK# de-assertion. Inside these undefined regions the PBE# signal is driven. FERR# is driven at all other times.

Figure 2-21. VID Step Timings



Ta = T84: VID Down to Valid V_{CC}(max)
Tb = T82: VID Down to Valid V_{CC}(min)
Tc = T85: VID Up to Valid V_{CC}(max)
Td = T83: VID Up to Valid V_{CC}(min)

Figure 2-22. VID Step Times and V_{CC} Waveforms



Ta = T80: VID Step Time
Tb = T81: Thermal Monitor 2 Dwell Time
Tc = T84: VID Down to Valid V_{CC}(max)
Td = T82: VID Down to Valid V_{CC}(min)
Te = T85: VID Up to Valid V_{CC}(max)
Tf = T83: VID Up to Valid V_{CC}(min)

Note: This waveform illustrates an example of an Intel Thermal Monitor 2 transition or an Intel Enhanced SpeedStep transition that is **six** VID steps down from the current state and six steps back up. Any arbitrary up or down transition can be generalized from this waveform.

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3 Front Side Bus Signal Quality Specifications

Source synchronous data transfer requires the clean reception of data signals and their associated strobes. Ringing below receiver thresholds, non-monotonic signal edges, and excessive voltage swings will adversely affect system timings. Ringback and signal non-monotonicity cannot be tolerated since these phenomena may inadvertently advance receiver state machines. Excessive signal swings (overshoot and undershoot) are detrimental to silicon gate oxide integrity, and can cause device failure if absolute voltage limits are exceeded. Overshoot and undershoot can also cause timing degradation due to the build up of inter-symbol interference (ISI) effects. For these reasons, it is crucial that the designer work towards a solution that provides acceptable signal quality across all systematic variations encountered in volume manufacturing.

This section documents signal quality metrics used to derive topology and routing guidelines through simulation. All specifications are specified at the processor core (pad measurements).

Specifications for signal quality are for measurements at the processor core only and are only observable through simulation. The same is true for all front side bus AC timing specifications in Section 2.12. Therefore, proper simulation of the processor front side bus is the only way to verify proper timing and signal quality.

3.1 Front Side Bus Signal Quality Specifications and Measurement Guidelines

3.1.1 Ringback Guidelines

Many scenarios have been simulated to generate a set of AGTL+ layout guidelines.

Table 3-1 provides the signal quality specifications for the AGTL+ and GTL+ asynchronous signal groups. Table 3-2 demonstrates the signal quality specification for the TAP signal group. These specifications are for use in simulating signal quality at the processor pads.

Maximum allowable overshoot and undershoot specifications for a given duration of time are detailed in Table 3-3 through Section 3-6. front side bus ringback tolerance for AGTL+ and GTL+ asynchronous signal groups are shown in Figure 3-1 (low-to-high transitions) and Figure 3-2 (high-to-low transitions).

The TAP signal group includes hysteresis on the input buffers and thus has relaxed ringback requirements when compared to the other buffer types. Figure 3-3 shows the front side bus ringback tolerance for low-to-high transitions and Figure 3-4 for high-to-low transitions. The hysteresis values Vt+ and Vt- can be found in Table 2-16.

Table 3-1. Ringback Specifications for AGTL+ and GTL+ Asynchronous Signal Groups

Signal Group	Transition	Maximum Ringback (with Input Diodes Present)	Unit	Figure	Notes
AGTL+, Async GTL+	Low → High	GTLREF + (0.06 * V_{TT})	V	3-1	1,2,3,4,5,6
AGTL+, Async GTL+	High → Low	GTLREF - (0.06 * V_{TT})	V	3-2	1,2,3,4,5,6

NOTES:
1. All signal integrity specifications are measured at the processor core (pads).
2. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
3. Specifications are for the edge rate of 1.8- 2.2V/ns.
4. All values specified by design characterization.
5. Please see Section 3.1.3 for maximum allowable overshoot.
6. The total ringback tolerance is 6% of V_{TT} (0.06 * V_{TT}). This consists of 4% AC and 2% DC components. Ringback between GTLREF + (0.06 * V_{TT}) and GTLREF - (0.06 * V_{TT}) is not supported.

Figure 3-1. Low-to-High Front Side Bus Receiver Ringback Tolerance

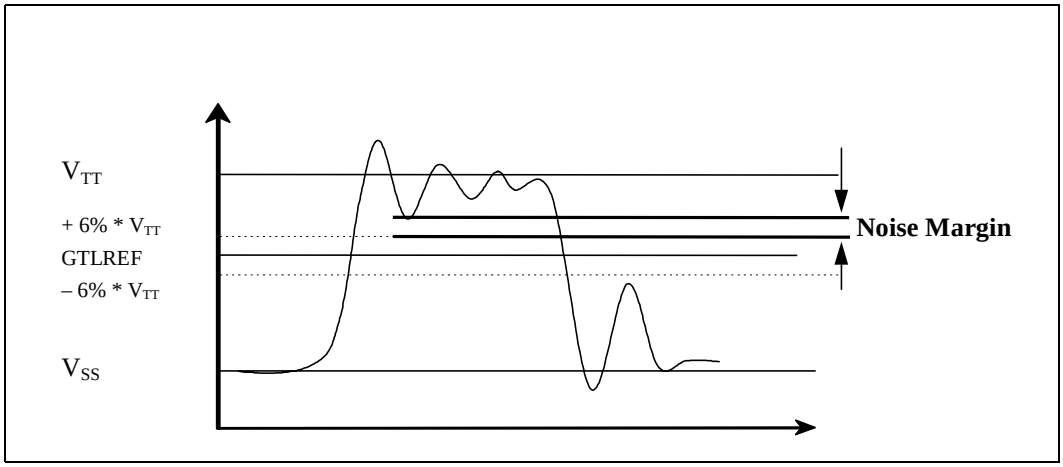


Figure 3-2. High-to-Low Front Side Bus Receiver Ringback Tolerance

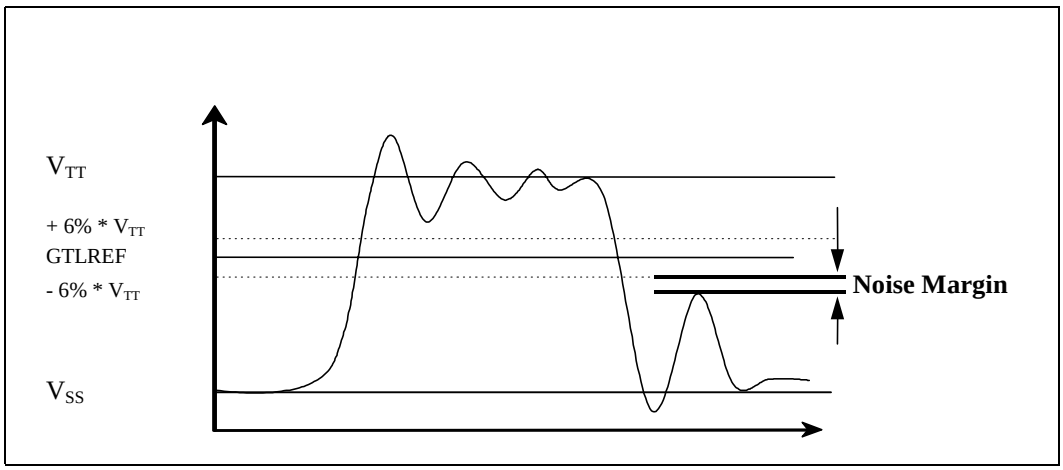


Table 3-2. Ringback Specifications for PWRGOOD and TAP Signal Groups

Signal Group	Transition	Maximum Ringback (with Input Diodes Present)	Unit	Figure	Notes
PWRGOOD and TAP	Low → High	$V_{t+(max)}$ to $V_{t-(max)}$	V	3-3	1,2,3,4
PWRGOOD and TAP	High → Low	$V_{t-(min)}$ to $V_{t+(min)}$	V	3-4	1,2,3,4

NOTES:
1. All signal integrity specifications are measured at the processor core (pads).
2. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
3. All values specified by design characterization.
4. Please see Section 3.1.3 for maximum allowable overshoot.

Figure 3-3. Low-to-High Receiver Ringback Tolerance for PWRGOOD and TAP Signals

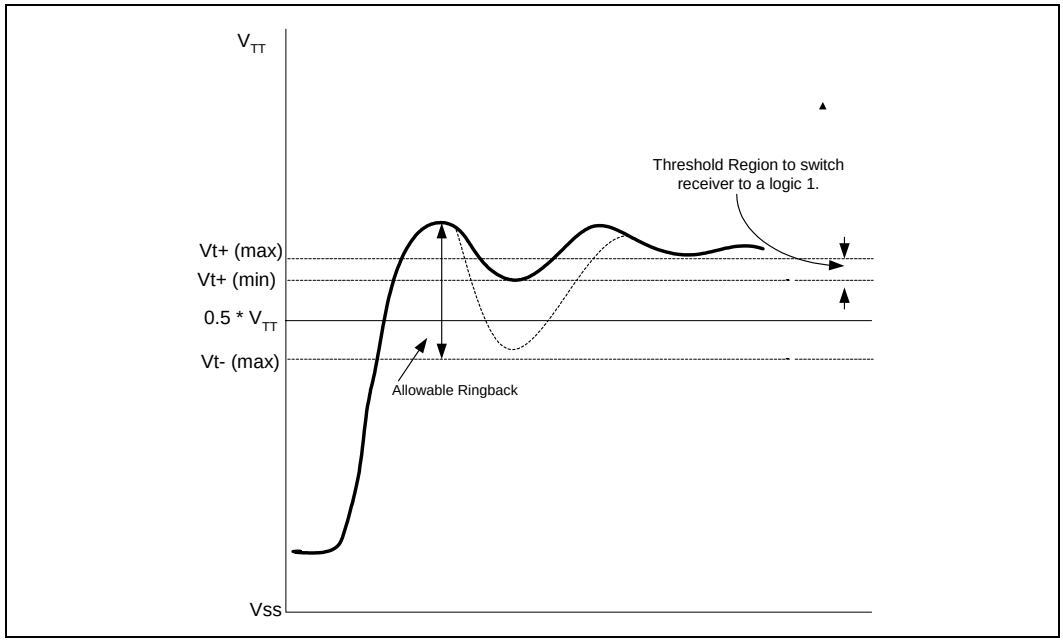
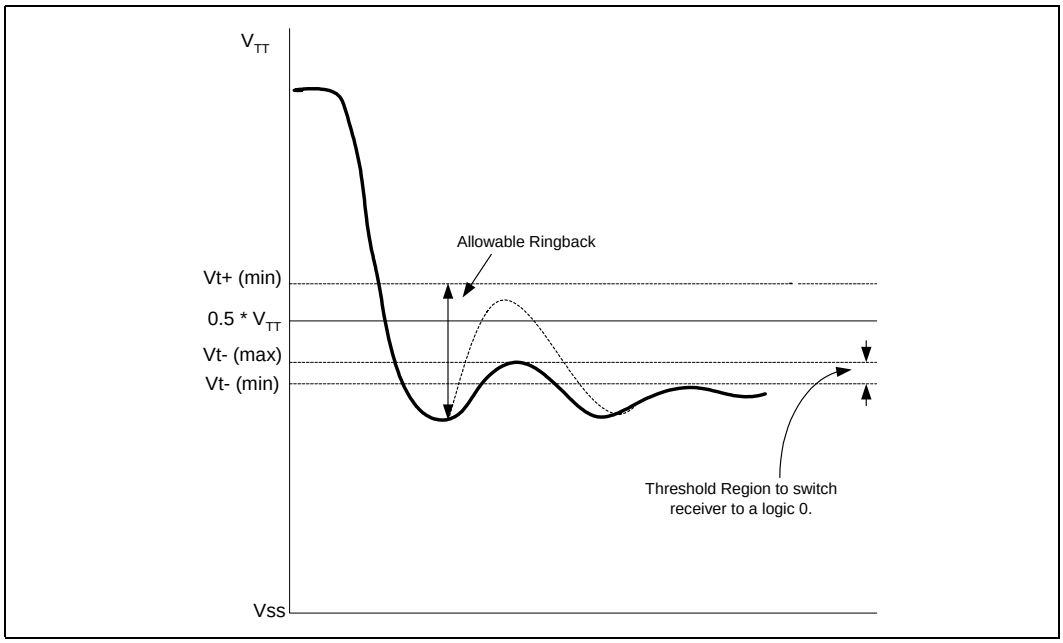


Figure 3-4. High-to-Low Receiver Ringback Tolerance for PWRGOOD and TAP Signals



3.1.2 Overshoot/Undershoot Guidelines

Overshoot (or undershoot) is the absolute value of the maximum voltage above or below V_{SS}. The overshoot/undershoot specifications limit transitions beyond V_{TT} or V_{SS} due to the fast signal edge rates. The processor can be damaged by single and/or repeated overshoot or undershoot events on any input, output, or I/O buffer if the charge is large enough (i.e., if the over/undershoot is great enough). Determining the impact of an overshoot/undershoot condition requires knowledge of the magnitude, the pulse duration, and the activity factor (AF). Permanent damage to the processor is the likely result of excessive overshoot/undershoot.

When performing simulations to determine the impact of overshoot and undershoot effects, ESD diodes must be properly characterized. ESD protection diodes do not act as voltage clamps and will not provide overshoot or undershoot protection. ESD diodes modeled within Intel signal integrity models do not clamp undershoot or overshoot and will yield correct simulation results. If other signal integrity models are being used to characterize the processor front side bus, care must be taken to ensure that ESD models do not clamp extreme voltage levels. Intel signal integrity models also contain I/O capacitance characterization. Therefore, removing the ESD diodes from a signal integrity model will impact results and may yield excessive overshoot/undershoot.

3.1.3 Overshoot/Undershoot Magnitude

Magnitude describes the maximum potential difference between a signal and its voltage reference level. For the processor, both are referenced to V_{SS}. It is important to note that overshoot and undershoot conditions are separate and their impact must be determined independently.

The pulse magnitude, duration, and activity factor must all be used to determine if the overshoot/undershoot pulse is within specifications.

3.1.4 Overshoot/Undershoot Pulse Duration

Pulse duration describes the total amount of time that an overshoot/undershoot event exceeds the overshoot/undershoot reference voltage. The total time could encompass several oscillations above the reference voltage. Multiple overshoot/undershoot pulses within a single overshoot/undershoot event may need to be measured to determine the total pulse duration.

Note: Oscillations below the reference voltage cannot be subtracted from the total overshoot/undershoot pulse duration.

3.1.5 Activity Factor

Activity Factor (AF) describes the frequency of overshoot (or undershoot) occurrence relative to a clock. Since the highest frequency of assertion of any common clock signal is every other clock, an AF = 1 indicates that the specific overshoot (or undershoot) waveform occurs every other clock cycle. Thus, an AF = 0.01 indicates that the specific overshoot (or undershoot) waveform occurs one time in every 200 clock cycles.

For source synchronous signals (address, data, and associated strobes), the activity factor is in reference to the strobe edge. The highest frequency of assertion of any source synchronous signal is every active edge of its associated strobe. So, an AF = 1 indicates that the specific overshoot (or undershoot) waveform occurs every strobe cycle.

The specifications provided in Table 3-3 through Table 3-6 show the maximum pulse duration allowed for a given overshoot/undershoot magnitude at a specific activity factor. Each table entry is independent of all others (meaning that the pulse duration reflects the existence of overshoot/undershoot events of that magnitude ONLY). A platform with an overshoot/undershoot that just meets the pulse duration for a specific magnitude where the AF < 1 means that there can be no other overshoot/undershoot events, even of lesser magnitude (note that if AF = 1, then the event occurs at all times and no other events can occur).

Note 1: Activity factor for common clock AGTL+ signals is referenced to BCLK[1:0] frequency.

Note 2: Activity factor for source synchronous (2x) signals is referenced to ADSTB[1:0]#.

Note 3: Activity factor for source synchronous (4x) signals is referenced to DSTBP[3:0]# and DSTBN[3:0]#.

3.1.6 Reading Overshoot/Undershoot Specification Tables

The overshoot/undershoot specification for the processor is not a simple single value. Instead, many factors are needed to determine what the over/undershoot specification is. In addition to the magnitude of the overshoot, the following parameters must also be known: the width of the overshoot and the activity factor (AF). To determine the allowed overshoot for a particular overshoot event, the following must be done:

1. Determine the *signal group* that particular signal falls into. For AGTL+ signals operating in the 4x source synchronous domain, use Table 3-3. For AGTL+ signals operating in the 2x source synchronous domain, use Table 3-4. If the signal is an AGTL+ signal operating in the common clock domain, use Table 3-5. Finally, all other signals are referenced in Table 3-6.
2. Determine the *magnitude* of the overshoot or the undershoot (relative to V_{SS}).
3. Determine the *activity factor* (how often does this overshoot occurs).

4. Next, from the appropriate specification table, determine the *maximum pulse duration* (in nanoseconds) allowed.
5. Compare the specified maximum pulse duration to the signal being measured. If the pulse duration measured is less than the pulse duration shown in the table, then the signal meets the specifications.

Undershoot events must be analyzed separately from overshoot events as they are mutually exclusive.

3.1.7 Determining if a System Meets Over/Undershoot Specifications

The overshoot/undershoot specifications listed in the following tables specify the allowable overshoot/undershoot for a single overshoot/undershoot event. Most systems will have multiple overshoot and/or undershoot events that each have their own set of parameters (duration, AF and magnitude). While each overshoot on its own may meet the overshoot specification, evaluate the cumulative overshoot of every cycle. A guideline to ensure a system passes the overshoot and undershoot specifications is shown below. Results from simulation may also be evaluated by utilizing the appropriate *Processor Overshoot Checker Tool* through the use of time-voltage data files.

1. If only one overshoot/undershoot event magnitude occurs, ensure it meets the over/undershoot specifications in the following tables OR
2. If multiple overshoots and/or multiple undershoots occur, measure the worst case pulse duration for each magnitude and compare the results against the AF = 1 specifications. If all of these worst case overshoot or undershoot events meet the specifications (measured time < specifications) in the table (where AF=1), then the system passes.

Note: The following notes apply to Table 3-3 through Table 3-6.

1. Absolute Maximum Overshoot is measured referenced to V_{SS}. Pulse Duration of overshoot is measured relative to V_{TT}.
2. Absolute Maximum Undershoot and Pulse Duration of undershoot is measured relative to V_{SS}.
3. Ringback below V_{TT} cannot be subtracted from overshoots/undershoots.
4. Lesser undershoot does not allocate longer or larger overshoot.
5. OEM's are strongly encouraged to follow Intel layout recommendations.
6. All values specified by design characterization.

Table 3-3. Source Synchronous (667MHz) AGTL+ Signals Over/Undershoot Tolerance

Absolute Maximum Overshoot (V)	Absolute Maximum Undershoot (V)	Pulse Duration (ns) AF = 1	Pulse Duration (ns) AF = 0.1
1.55	-0.35	0	0.2
1.50	-0.30	0	0.7
1.45	-0.25	0.1	1.5
1.40	-0.20	0.5	1.5
1.35	-0.15	1.3	1.5
1.30	-0.10	1.5	1.5

NOTES:
1. These specifications are measured at the processor pad.
2. Assumes a BCLK period of 6 ns.
3. AF is referenced to associated source synchronous strobes

Table 3-4. Source Synchronous (333 MHz) AGTL+ Signals Over/Undershoot Tolerance

Absolute Maximum Overshoot (V)	Absolute Maximum Undershoot (V)	Pulse Duration (ns) AF = 1	Pulse Duration (ns) AF = 0.1
1.55	-0.35	0	0.6
1.50	-0.30	0.1	1.9
1.45	-0.25	0.5	3.0
1.40	-0.20	1.3	3.0
1.35	-0.15	3.0	3.0
1.30	-0.10	3.0	3.0

NOTES:
1. These specifications are measured at the processor pad.
2. BCLK period is 6 ns.
3. AF is referenced to associated source synchronous strobe.

Table 3-5. Common Clock (166 MHz) AGTL+ Signals Overshoot/Undershoot Tolerance

Absolute Maximum Overshoot (V)	Absolute Maximum Undershoot (V)	Pulse Duration (ns) AF = 1	Pulse Duration (ns) AF = 0.1
1.55	-0.35	0.1	1.1
1.50	-0.30	0.3	3.2
1.45	-0.25	0.8	6.0
1.40	-0.20	2.3	6.0
1.35	-0.15	6.0	6.0
1.30	-0.10	6.0	6.0

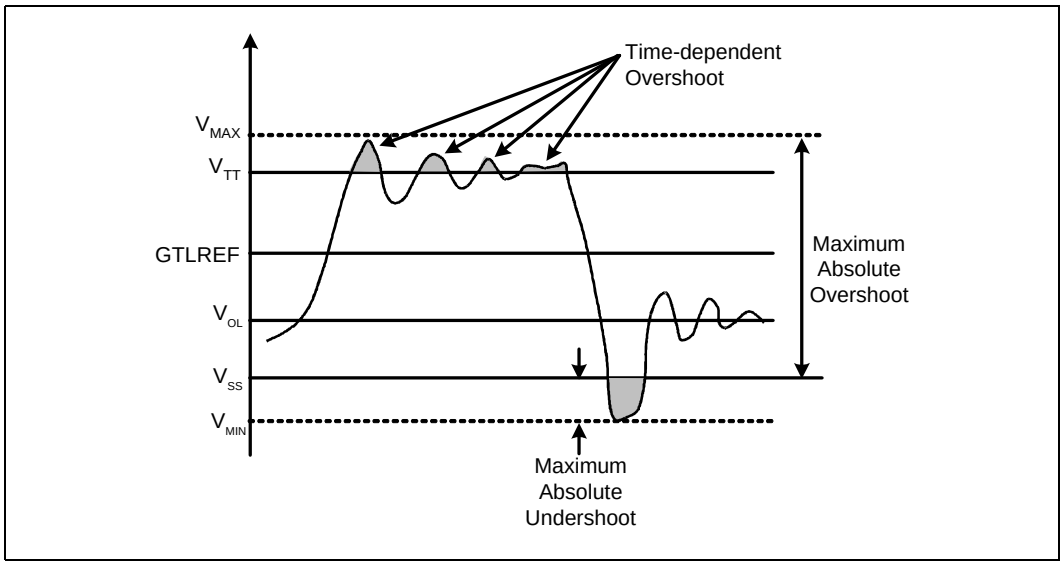
NOTES:
1. These specifications are measured at the processor pad.
2. BCLK period is 6 ns.
3. AF is referenced to BCLK[1:0]

Table 3-6. GTL+ Asynchronous, PWRGOOD, TAP Signals Over/Undershoot Tolerance

Absolute Maximum Overshoot (V)	Absolute Maximum Undershoot (V)	Pulse Duration (ns) AF = 1	Pulse Duration (ns) AF = 0.1
1.55	-0.35	0.4	4.7
1.50	-0.30	1.3	12.8
1.45	-0.25	3.4	30.0
1.40	-0.20	9.3	30.0
1.35	-0.15	25.0	30.0
1.30	-0.10	30.0	30.0

NOTES:
1. These specifications are measured at the processor pad.
2. AF is referenced to a 33 MHz time domain.

Figure 3-5. Maximum Acceptable Overshoot/Undershoot Waveform



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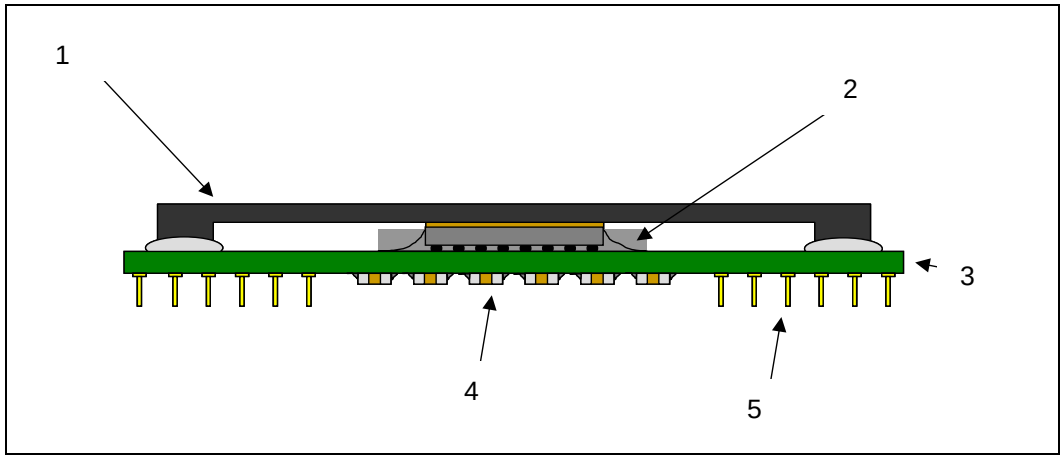
4 Mechanical Specifications

The 64-bit Intel® Xeon™ processor MP with up to 8MB L3 cache is packaged in a Flip-Chip Micro Pin Grid Array 4 (FC-mPGA4) package that interfaces with the motherboard via a mPGA604 socket. The package consists of a processor core mounted on a substrate pin-carrier. An integrated heat spreader (IHS) is attached to the package substrate and core and serves as the mating surface for processor component thermal solutions, such as a heatsink. Figure 4-1 shows a sketch of the processor package components and how they are assembled together.

The package components shown in Figure 4-1 include the following:

1. Integrated Heat Spreader (IHS)
2. Processor die
3. FC-mPGA4 package
4. Pin-side capacitors
5. Package pin

Figure 4-1. Processor Package Assembly Sketch



Note: This drawing is not to scale and is for reference only. The mPGA604 socket is not shown.

4.1 Package Mechanical Drawing

The package mechanical drawings are shown in Figure 4-2 and Figure 4-3. The drawings include dimensions necessary to design a thermal solution for the processor. These dimensions include:

1. Package reference with tolerances (total height, length, width, etc.)
2. IHS parallelism and tilt
3. Pin dimensions
4. Top-side and back-side component keep-out dimensions
5. Reference datums

All drawing dimensions are in mm[in].

Figure 4-2. Processor Package Drawing (Sheet 1 of 2)

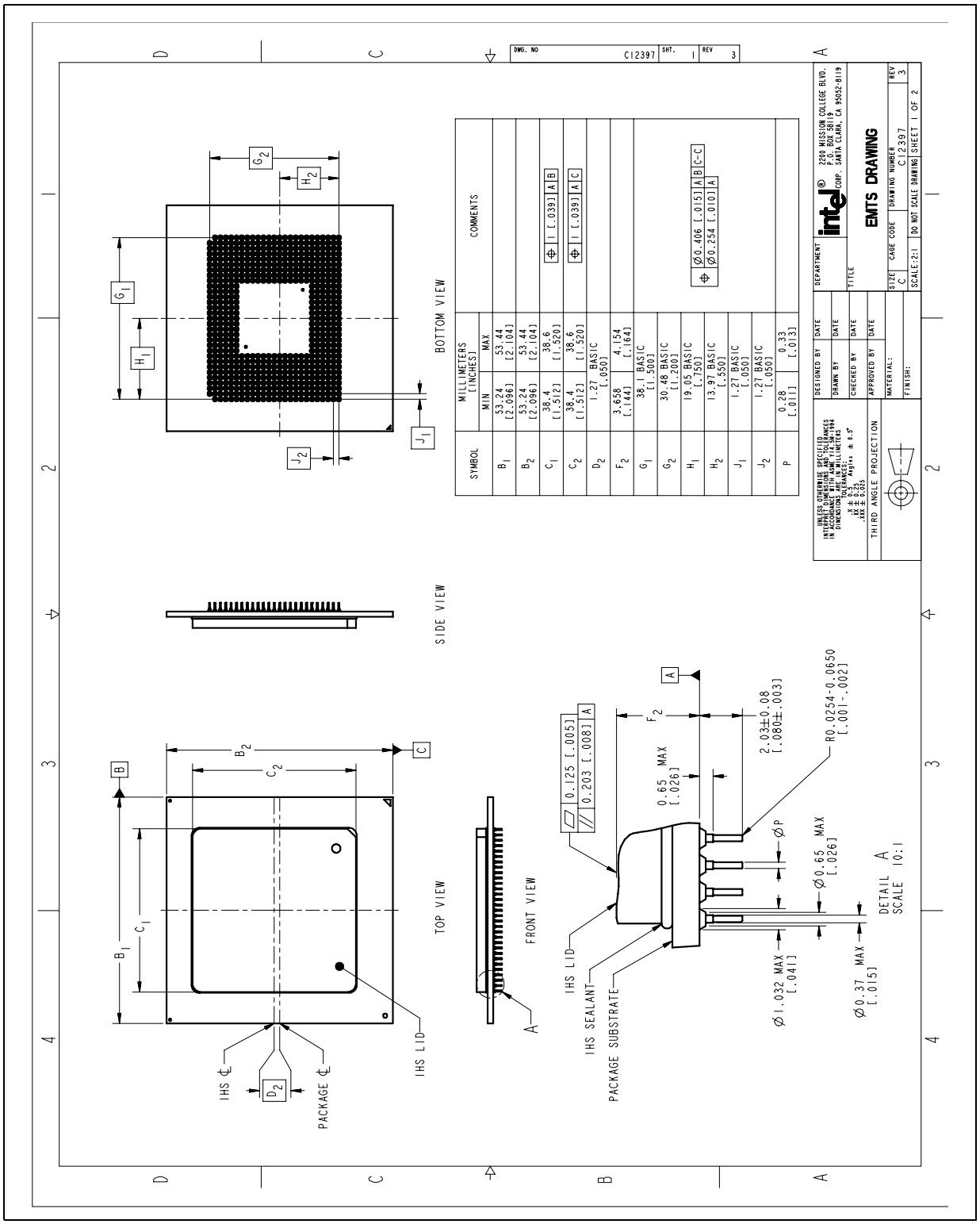
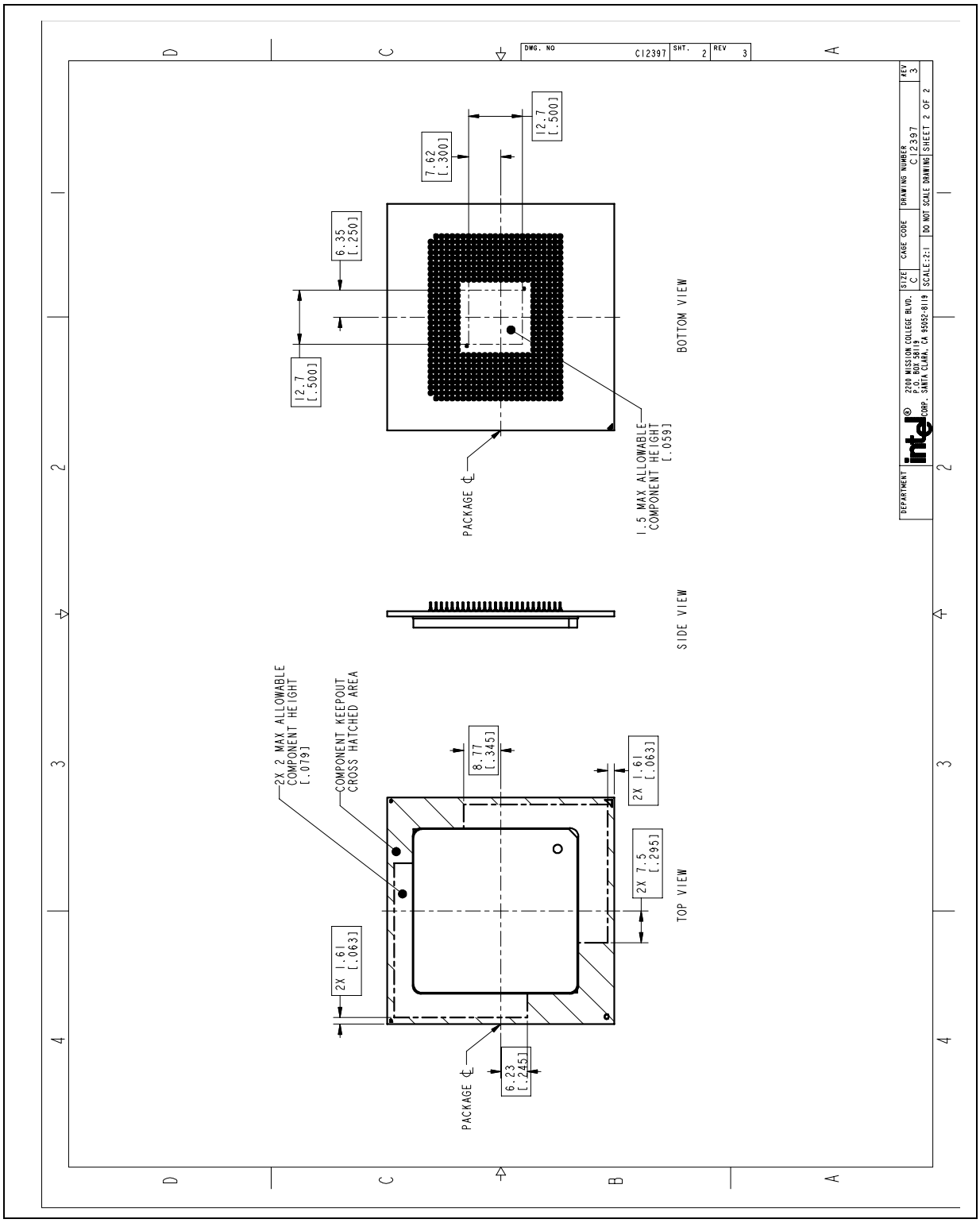


Figure 4-3. Processor Package Drawing (Sheet 2 of 2)



4.2 Processor Component Keep-Out Zones

The processor may contain components on the substrate that define component keep-out zone requirements. A thermal and mechanical solution design must not intrude into the required keep-out zones. Decoupling capacitors are typically mounted to either the topside or pin-side of the package substrate. See Figure 4-2 and Figure 4-3 for keepout zones.

4.3 Package Loading Specifications

Table 4-1 provides dynamic and static load specifications for the processor package. These mechanical load limits should not be exceeded during heatsink assembly, shipping conditions, or standard use condition. Also, any mechanical system or component testing should not exceed the maximum limits. The processor package substrate should not be used as a mechanical reference or load-bearing surface for thermal and mechanical solutions. The minimum loading specification must be maintained by any thermal and mechanical solution.

Table 4-1. Processor Loading Specifications

Parameter	Minimum	Maximum	Unit	Notes
Static Compressive Load	44 10	222 50	N lbf	1, 2, 3, 4
	44 10	288 65	N lbf	1, 2, 3, 5
Dynamic Compressive Load		222 N + 0.45 kg * 100 G 50 lbf (static) + 1 lbm * 100 G	N lbf	1, 3, 4, 6, 7
		288 N + 0.45 kg * 100 G 65 lbf (static) + 1 lbm * 100 G	N lbf	1, 3, 5, 6, 7
Transient		445 100	N lbf	1, 3, 8

NOTES:
1. These specifications apply to uniform compressive loading in a direction perpendicular to the IHS top surface.
2. This is the minimum and maximum static force that can be applied by the heatsink and retention solution to maintain the heatsink and processor interface.
3. These parameters are based on limited testing for design characterization. Loading limits are for the package only and do not include the limits of the processor socket.
4. This specification applies for thermal retention solutions that allow baseboard deflection.
5. This specification applies either for thermal retention solutions that prevent baseboard deflection or for the Intel enabled reference solution.
6. Dynamic loading is defined as an 11 ms duration average load superimposed on the static load requirement.
7. Experimentally validated test condition used a heatsink mass of 1 lbm (~0.45 kg) with 100 G acceleration measured at heatsink mass. The dynamic portion of this specification in the product application can have flexibility in specific values, but the ultimate product of mass times acceleration should not exceed this validated dynamic load (1 lbm x 100 G = 100 lb).
8. Transient loading is defined as a 2 second duration peak load superimposed on the static load requirement, representative of loads experienced by the package during heatsink installation.

4.4 Package Handling Guidelines

Table 4-2 includes a list of guidelines on package handling in terms of recommended maximum loading on the processor IHS relative to a fixed substrate. These package handling loads may be experienced during heatsink removal.

Table 4-2. Package Handling Guidelines

Parameter	Maximum Recommended	Notes
Shear	356 N [80 lbf]	1, 4, 5
Tensile	156 N [35 lbf]	2, 4, 5
Torque	8 N-m [70 lbf-in]	3, 4, 5

NOTES:
1. A shear load is defined as a load applied to the IHS in a direction parallel to the IHS top surface.
2. A tensile load is defined as a pulling load applied to the IHS in the direction normal to the IHS surface.
3. A torque load is defined as a twisting load applied to the IHS in an axis of rotation normal to the IHS top surface.
4. These guidelines are based on limited testing for design characterization and incidental applications (one time only).
5. Handling guidelines are for the package only and do not include the limits of the processor socket.

4.5 Package Insertion Specifications

The processor can be inserted into and removed from a mPGA604 socket 15 times. The socket should meet the mPGA604 requirements detailed in the *mPGA604 Socket Design Guidelines*.

4.6 Processor Mass Specifications

The typical mass of the processor is 34 g [1.20 oz]. This mass [weight] includes all the components that are included in the package.

4.7 Processor Materials

Table 4-3 lists some of the package components and associated materials.

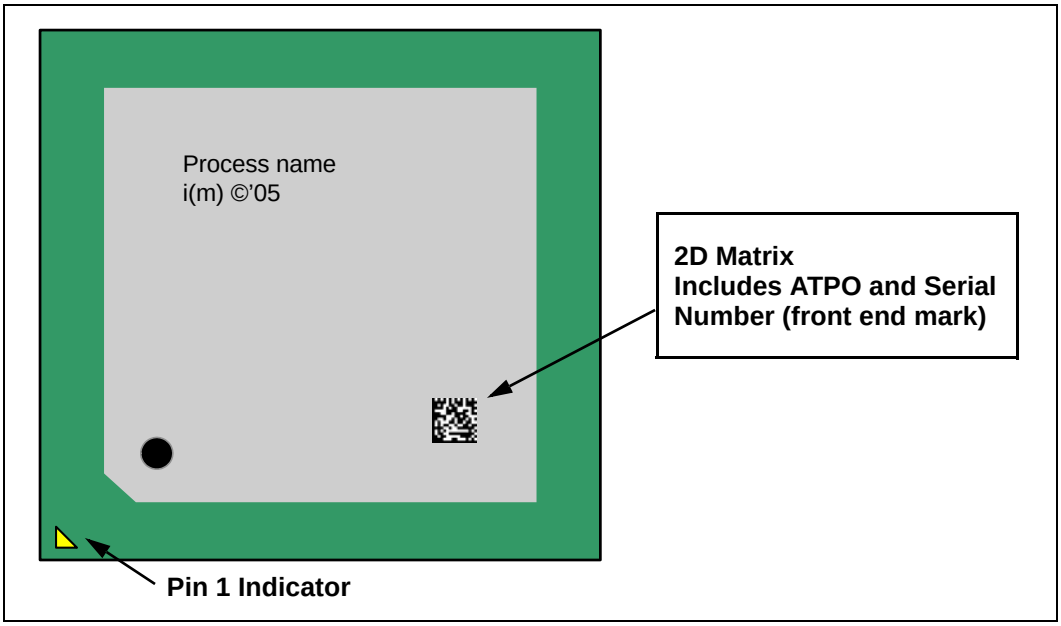
Table 4-3. Processor Materials

Component	Material
Integrated Heat Spreader (IHS)	Nickel Plated Copper
Substrate	Fiber-Reinforced Resin
Substrate Pins	Gold Plated Copper

4.8 Processor Markings

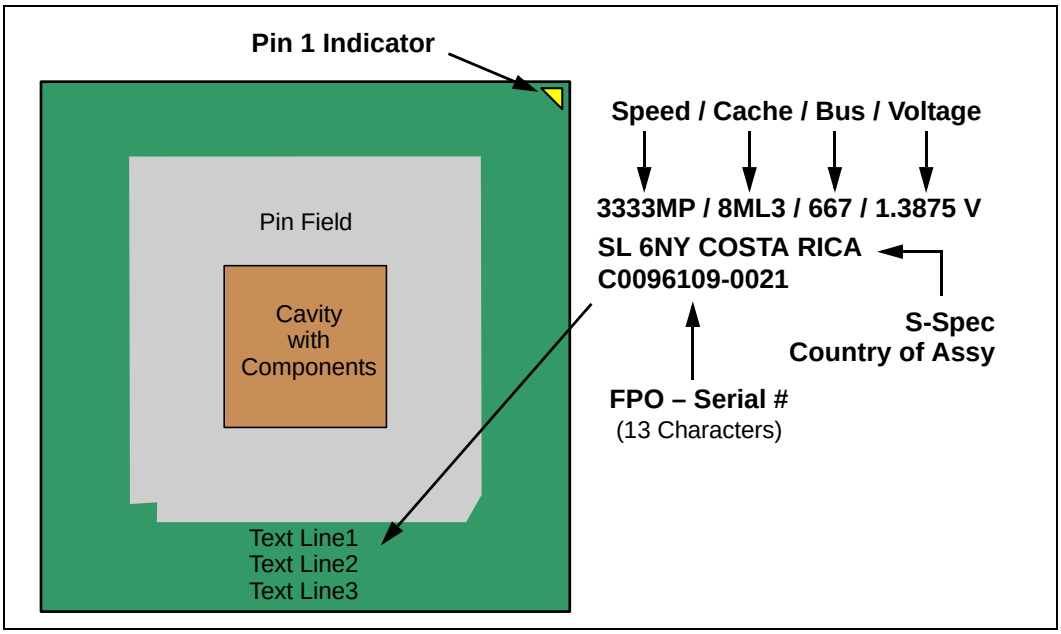
Figure 4-4 shows the topside markings and Figure 4-5 shows the bottom-side markings on the processor. These diagrams are to aid in the identification of the processor.

Figure 4-4. Processor Topside Markings



NOTES:
1. All characters will be in upper case.
2. Drawing is not to scale.

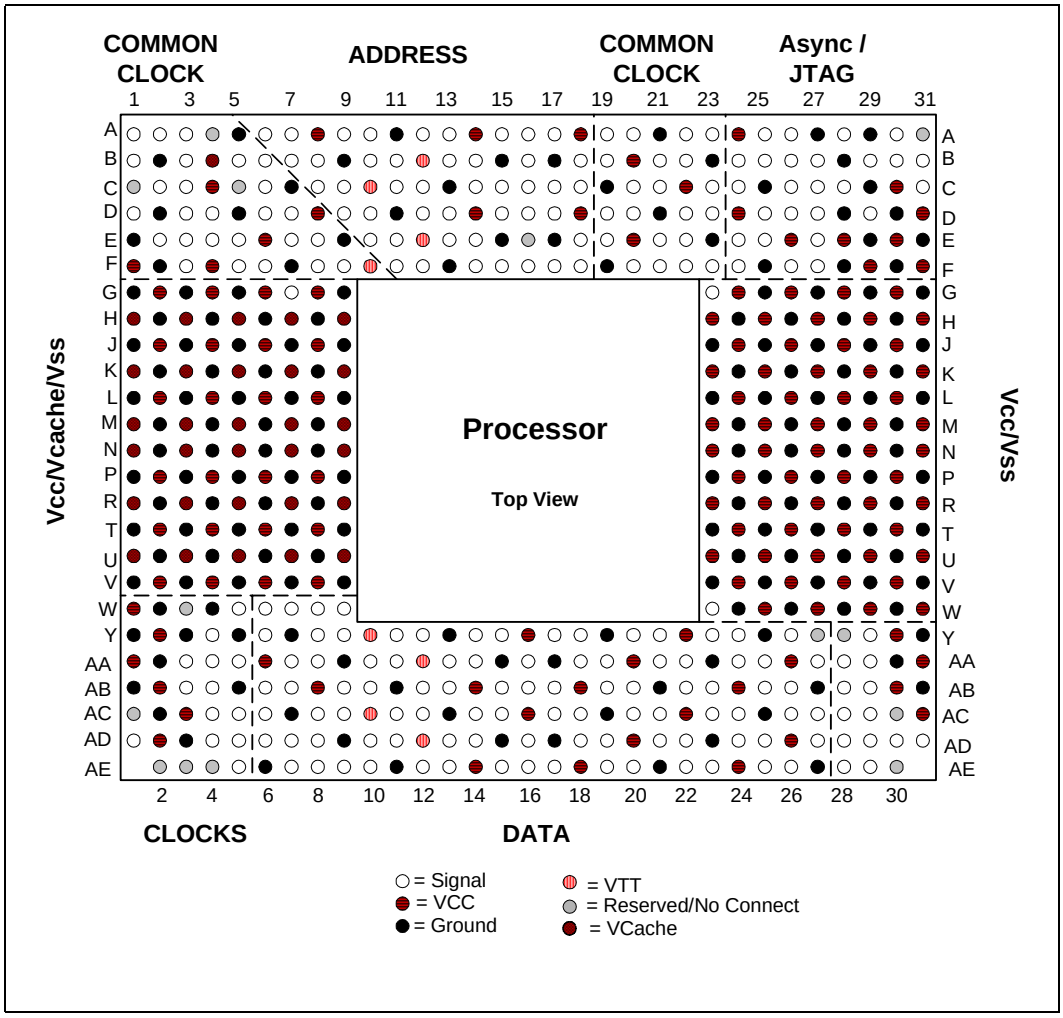
Figure 4-5. Processor Bottom-Side Markings



4.9 Processor Pin-Out Coordinates

Figure 4-6 shows the top view of the processor pin coordinates. The coordinates are referred to throughout the document to identify processor pins.

Figure 4-6. Processor Pin-Out Coordinates, Top View



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5 Pin Listing

5.1 Processor Pin Assignments

Section 2.6 contains the front side bus signal groups for the processor (see Table 2-5). This section provides a sorted pin list in Table 5-1 and Table 5-2. Table 5-1 is a listing of all processor pins ordered alphabetically by pin name. Table 5-2 is a listing of all processor pins ordered by pin number.

5.1.1 Pin Listing by Pin Name

Table 5-1. Pin Listing by Pin Name

Pin Name	Pin No.	Signal Buffer Type	Direction
A3#	A22	Source Sync	Input/Output
A4#	A20	Source Sync	Input/Output
A5#	B18	Source Sync	Input/Output
A6#	C18	Source Sync	Input/Output
A7#	A19	Source Sync	Input/Output
A8#	C17	Source Sync	Input/Output
A9#	D17	Source Sync	Input/Output
A10#	A13	Source Sync	Input/Output
A11#	B16	Source Sync	Input/Output
A12#	B14	Source Sync	Input/Output
A13#	B13	Source Sync	Input/Output
A14#	A12	Source Sync	Input/Output
A15#	C15	Source Sync	Input/Output
A16#	C14	Source Sync	Input/Output
A17#	D16	Source Sync	Input/Output
A18#	D15	Source Sync	Input/Output
A19#	F15	Source Sync	Input/Output
A20#	A10	Source Sync	Input/Output
A21#	B10	Source Sync	Input/Output
A22#	B11	Source Sync	Input/Output
A23#	C12	Source Sync	Input/Output
A24#	E14	Source Sync	Input/Output
A25#	D13	Source Sync	Input/Output
A26#	A9	Source Sync	Input/Output
A27#	B8	Source Sync	Input/Output

Table 5-1. Pin Listing by Pin Name (cont'd)

Pin Name	Pin No.	Signal Buffer Type	Direction
A28#	E13	Source Sync	Input/Output
A29#	D12	Source Sync	Input/Output
A30#	C11	Source Sync	Input/Output
A31#	B7	Source Sync	Input/Output
A32#	A6	Source Sync	Input/Output
A33#	A7	Source Sync	Input/Output
A34#	C9	Source Sync	Input/Output
A35#	C8	Source Sync	Source Sync
A36#	F16	Source Sync	Source Sync
A37#	F22	Source Sync	Source Sync
A38#	B6	Source Sync	Source Sync
A39#	C16	Source Sync	Source Sync
A20M#	F27	Async GTL+	Input
ADS#	D19	Common Clk	Input/Output
ADSTB0#	F17	Source Sync	Input/Output
ADSTB1#	F14	Source Sync	Input/Output
AP0#	E10	Common Clk	Input/Output
AP1#	D9	Common Clk	Input/Output
BCLK0	Y4	FSB Clk	Input
BCLK1	W5	FSB Clk	Input
BINIT#	F11	Common Clk	Input/Output
BNR#	F20	Common Clk	Input/Output

Table 5-1. Pin Listing by Pin Name (cont'd)

Pin Name	Pin No.	Signal Buffer Type	Direction
BOOT_SELECT	G7	Power/Other	Input
BPM0#	F6	Common Clk	Input/Output
BPM1#	F8	Common Clk	Input/Output
BPM2#	E7	Common Clk	Input/Output
BPM3#	F5	Common Clk	Input/Output
BPM4#	E8	Common Clk	Input/Output
BPM5#	E4	Common Clk	Input/Output
BPRI#	D23	Common Clk	Input
BR0#	D20	Common Clk	Input/Output
BR1#	F12	Common Clk	Input
BR2#[1]	E11	Common Clk	Input
BR3#[1]	D10	Common Clk	Input
BSEL0	AA3	Power/Other	Output
BSEL1	AB3	Power/Other	Output
COMP0	AD16	Power/Other	Input
CVID0	E2	Power/Other	Output
CVID1	D1	Power/Other	Output
CVID2	C2	Power/Other	Output
CVID3	A2	Power/Other	Output
D0#	Y26	Source Sync	Input/Output
D1#	AA27	Source Sync	Input/Output
D2#	Y24	Source Sync	Input/Output
D3#	AA25	Source Sync	Input/Output
D4#	AD27	Source Sync	Input/Output
D5#	Y23	Source Sync	Input/Output
D6#	AA24	Source Sync	Input/Output
D7#	AB26	Source Sync	Input/Output
D8#	AB25	Source Sync	Input/Output
D9#	AB23	Source Sync	Input/Output
D10#	AA22	Source Sync	Input/Output
D11#	AA21	Source Sync	Input/Output
D12#	AB20	Source Sync	Input/Output
D13#	AB22	Source Sync	Input/Output
D14#	AB19	Source Sync	Input/Output
D15#	AA19	Source Sync	Input/Output
D16#	AE26	Source Sync	Input/Output
D17#	AC26	Source Sync	Input/Output

Table 5-1. Pin Listing by Pin Name (cont'd)

Pin Name	Pin No.	Signal Buffer Type	Direction
D18#	AD25	Source Sync	Input/Output
D19#	AE25	Source Sync	Input/Output
D20#	AC24	Source Sync	Input/Output
D21#	AD24	Source Sync	Input/Output
D22#	AE23	Source Sync	Input/Output
D23#	AC23	Source Sync	Input/Output
D24#	AA18	Source Sync	Input/Output
D25#	AC20	Source Sync	Input/Output
D26#	AC21	Source Sync	Input/Output
D27#	AE22	Source Sync	Input/Output
D28#	AE20	Source Sync	Input/Output
D29#	AD21	Source Sync	Input/Output
D30#	AD19	Source Sync	Input/Output
D31#	AB17	Source Sync	Input/Output
D32#	AB16	Source Sync	Input/Output
D33#	AA16	Source Sync	Input/Output
D34#	AC17	Source Sync	Input/Output
D35#	AE13	Source Sync	Input/Output
D36#	AD18	Source Sync	Input/Output
D37#	AB15	Source Sync	Input/Output
D38#	AD13	Source Sync	Input/Output
D39#	AD14	Source Sync	Input/Output
D40#	AD11	Source Sync	Input/Output
D41#	AC12	Source Sync	Input/Output
D42#	AE10	Source Sync	Input/Output
D43#	AC11	Source Sync	Input/Output
D44#	AE9	Source Sync	Input/Output
D45#	AD10	Source Sync	Input/Output
D46#	AD8	Source Sync	Input/Output
D47#	AC9	Source Sync	Input/Output
D48#	AA13	Source Sync	Input/Output
D49#	AA14	Source Sync	Input/Output
D50#	AC14	Source Sync	Input/Output
D51#	AB12	Source Sync	Input/Output
D52#	AB13	Source Sync	Input/Output
D53#	AA11	Source Sync	Input/Output
D54#	AA10	Source Sync	Input/Output

Table 5-1. Pin Listing by Pin Name (cont'd)

Pin Name	Pin No.	Signal Buffer Type	Direction
D55#	AB10	Source Sync	Input/Output
D56#	AC8	Source Sync	Input/Output
D57#	AD7	Source Sync	Input/Output
D58#	AE7	Source Sync	Input/Output
D59#	AC6	Source Sync	Input/Output
D60#	AC5	Source Sync	Input/Output
D61#	AA8	Source Sync	Input/Output
D62#	Y9	Source Sync	Input/Output
D63#	AB6	Source Sync	Input/Output
DBI0#	AC27	Source Sync	Input/Output
DBI1#	AD22	Source Sync	Input/Output
DBI2#	AE12	Source Sync	Input/Output
DBI3#	AB9	Source Sync	Input/Output
DBSY#	F18	Common Clk	Input/Output
DEFER#	C23	Common Clk	Input
DEP0#	AD31	Source Sync	Input/Output
DEP1#	AD30	Source Sync	Input/Output
DEP2#	AE16	Source Sync	Input/Output
DEP3#	AE15	Source Sync	Input/Output
DEP4#	AE8	Source Sync	Input/Output
DEP5#	AD6	Source Sync	Input/Output
DEP6#	AC4	Source Sync	Input/Output
DEP7#	AA4	Source Sync	Input/Output
DP0#	AC18	Common Clk	Input/Output
DP1#	AE19	Common Clk	Input/Output
DP2#	AC15	Common Clk	Input/Output
DP3#	AE17	Common Clk	Input/Output
DRDY#	E18	Common Clk	Input/Output
DSTBN0#	Y21	Source Sync	Input/Output
DSTBN1#	Y18	Source Sync	Input/Output
DSTBN2#	Y15	Source Sync	Input/Output
DSTBN3#	Y12	Source Sync	Input/Output
DSTBP0#	Y20	Source Sync	Input/Output
DSTBP1#	Y17	Source Sync	Input/Output
DSTBP2#	Y14	Source Sync	Input/Output
DSTBP3#	Y11	Source Sync	Input/Output
FERR#/PBE#	E27	Async GTL+	Output

Table 5-1. Pin Listing by Pin Name (cont'd)

Pin Name	Pin No.	Signal Buffer Type	Direction
FORCEPR#	A15	Power/Other	Input
GTLREF0	W23	Power/Other	Input
GTLREF1	W9	Power/Other	Input
GTLREF2	F23	Power/Other	Input
GTLREF3	F9	Power/Other	Input
HIT#	E22	Common Clk	Input/Output
HITM#	A23	Common Clk	Input/Output
ID0#	A26	Common Clk	Input
ID1#	B26	Common Clk	Input
ID2#	D25	Common Clk	Input
ID3#	D27	Common Clk	Input
ID4#	C28	Common Clk	Input
ID5#	B29	Common Clk	Input
ID6#	B30	Common Clk	Input
ID7#	A30	Common Clk	Input
IDS#	A28	Common Clk	Input
IERR#	E5	Async GTL+	Output
IGNNE#	C26	Async GTL+	Input
INIT#	D6	Async GTL+	Input
LINT0/INTR	B24	Async GTL+	Input
LINT1/NMI	G23	Async GTL+	Input
LOCK#	A17	Common Clk	Input/Output
MCERR#	D7	Common Clk	Input/Output
ODTEN	B5	Power/Other	Input
OOD#	D29	Common Clk	Input
PROCHOT#	B25	Async GTL+	Output
PWRGOOD	AB7	Async GTL+	Input
REQ0#	B19	Source Sync	Input/Output
REQ1#	B21	Source Sync	Input/Output
REQ2#	C21	Source Sync	Input/Output
REQ3#	C20	Source Sync	Input/Output
REQ4#	B22	Source Sync	Input/Output
Reserved	A31		
Reserved	C1		
Reserved	E16		
Reserved	W3		
Reserved	Y27		

Table 5-1. Pin Listing by Pin Name (cont'd)

Pin Name	Pin No.	Signal Buffer Type	Direction
Reserved	Y28		
Reserved	AC1		
Reserved	AE4		
Reserved	AE30		
RESET#	Y8	Common Clk	Input
RS0#	E21	Common Clk	Input
RS1#	D22	Common Clk	Input
RS2#	F21	Common Clk	Input
RSP#	C6	Common Clk	Input
SKTOCC#	A3	Power/Other	Output
SLEW_CTRL	AC30	Power/Other	Input
SM_ALERT#	AD28	SMBus	Output
SM_CLK	AC28	SMBus	Input
SM_DAT	AC29	SMBus	Input/Output
SM_EP_A0	AA29	SMBus	Input
SM_EP_A1	AB29	SMBus	Input
SM_EP_A2	AB28	SMBus	Input
SM_TS1_A0	AA28	SMBus	Input
SM_TS1_A1	Y29	SMBus	Input
SM_VCC	AE28	Power/Other	
SM_VCC	AE29	Power/Other	
SM_WP	AD29	SMBus	Input
SMI#	C27	Async GTL+	Input
STPCLK#	D4	Async GTL+	Input
TCK	E24	TAP	Input
TDI	C24	TAP	Input
TDO	E25	TAP	Output
TEST_BUS	A16	Power/Other	Input
TESTHI0	W6	Power/Other	Input
TESTHI1	W7	Power/Other	Input
TESTHI2	W8	Power/Other	Input
TESTHI3	Y6	Power/Other	Input
TESTHI4	AA7	Power/Other	Input
TESTHI5	AD5	Power/Other	Input
TESTHI6	AE5	Power/Other	Input
THERMTRIP#	F26	Async GTL+	Output
TMS	A25	TAP	Input

Table 5-1. Pin Listing by Pin Name (cont'd)

Pin Name	Pin No.	Signal Buffer Type	Direction
TRDY#	E19	Common Clk	Input
TRST#	F24	TAP	Input
V_{CACHE}	B4	Power/Other	
V_{CACHE}	H1	Power/Other	
V_{CACHE}	H3	Power/Other	
V_{CACHE}	H5	Power/Other	
V_{CACHE}	H7	Power/Other	
V_{CACHE}	H9	Power/Other	
V_{CACHE}	K1	Power/Other	
V_{CACHE}	K3	Power/Other	
V_{CACHE}	K5	Power/Other	
V_{CACHE}	K7	Power/Other	
V_{CACHE}	K9	Power/Other	
V_{CACHE}	M1	Power/Other	
V_{CACHE}	M3	Power/Other	
V_{CACHE}	M5	Power/Other	
V_{CACHE}	M7	Power/Other	
V_{CACHE}	M9	Power/Other	
V_{CACHE}	N1	Power/Other	
V_{CACHE}	N3	Power/Other	
V_{CACHE}	N5	Power/Other	
V_{CACHE}	N7	Power/Other	
V_{CACHE}	N9	Power/Other	
V_{CACHE}	R1	Power/Other	
V_{CACHE}	R3	Power/Other	
V_{CACHE}	R5	Power/Other	
V_{CACHE}	R7	Power/Other	
V_{CACHE}	R9	Power/Other	
V_{CACHE}	U1	Power/Other	
V_{CACHE}	U3	Power/Other	
V_{CACHE}	U5	Power/Other	
V_{CACHE}	U7	Power/Other	
V_{CACHE}	U9	Power/Other	
V_{CC}	A8	Power/Other	
V_{CC}	A14	Power/Other	
V_{CC}	A18	Power/Other	
V_{CC}	A24	Power/Other	

Table 5-1. Pin Listing by Pin Name (cont'd)

Pin Name	Pin No.	Signal Buffer Type	Direction
V_{CC}	B20	Power/Other	
V_{CC}	C4	Power/Other	
V_{CC}	C22	Power/Other	
V_{CC}	C30	Power/Other	
V_{CC}	D8	Power/Other	
V_{CC}	D14	Power/Other	
V_{CC}	D18	Power/Other	
V_{CC}	D24	Power/Other	
V_{CC}	D31	Power/Other	
V_{CC}	E6	Power/Other	
V_{CC}	E20	Power/Other	
V_{CC}	E26	Power/Other	
V_{CC}	E28	Power/Other	
V_{CC}	E30	Power/Other	
V_{CC}	F1	Power/Other	
V_{CC}	F4	Power/Other	
V_{CC}	F29	Power/Other	
V_{CC}	F31	Power/Other	
V_{CC}	G2	Power/Other	
V_{CC}	G4	Power/Other	
V_{CC}	G6	Power/Other	
V_{CC}	G8	Power/Other	
V_{CC}	G24	Power/Other	
V_{CC}	G26	Power/Other	
V_{CC}	G28	Power/Other	
V_{CC}	G30	Power/Other	
V_{CC}	H23	Power/Other	
V_{CC}	H25	Power/Other	
V_{CC}	H27	Power/Other	
V_{CC}	H29	Power/Other	
V_{CC}	H31	Power/Other	
V_{CC}	J2	Power/Other	
V_{CC}	J4	Power/Other	
V_{CC}	J6	Power/Other	
V_{CC}	J8	Power/Other	
V_{CC}	J24	Power/Other	
V_{CC}	J26	Power/Other	

Table 5-1. Pin Listing by Pin Name (cont'd)

Pin Name	Pin No.	Signal Buffer Type	Direction
V_{CC}	J28	Power/Other	
V_{CC}	J30	Power/Other	
V_{CC}	K23	Power/Other	
V_{CC}	K25	Power/Other	
V_{CC}	K27	Power/Other	
V_{CC}	K29	Power/Other	
V_{CC}	K31	Power/Other	
V_{CC}	L2	Power/Other	
V_{CC}	L4	Power/Other	
V_{CC}	L6	Power/Other	
V_{CC}	L8	Power/Other	
V_{CC}	L24	Power/Other	
V_{CC}	L26	Power/Other	
V_{CC}	L28	Power/Other	
V_{CC}	L30	Power/Other	
V_{CC}	M23	Power/Other	
V_{CC}	M25	Power/Other	
V_{CC}	M27	Power/Other	
V_{CC}	M29	Power/Other	
V_{CC}	M31	Power/Other	
V_{CC}	N23	Power/Other	
V_{CC}	N25	Power/Other	
V_{CC}	N27	Power/Other	
V_{CC}	N29	Power/Other	
V_{CC}	N31	Power/Other	
V_{CC}	P2	Power/Other	
V_{CC}	P4	Power/Other	
V_{CC}	P6	Power/Other	
V_{CC}	P8	Power/Other	
V_{CC}	P24	Power/Other	
V_{CC}	P26	Power/Other	
V_{CC}	P28	Power/Other	
V_{CC}	P30	Power/Other	
V_{CC}	R23	Power/Other	
V_{CC}	R25	Power/Other	
V_{CC}	R27	Power/Other	
V_{CC}	R29	Power/Other	

Table 5-1. Pin Listing by Pin Name (cont'd)

Pin Name	Pin No.	Signal Buffer Type	Direction
V_{CC}	R31	Power/Other	
V_{CC}	T2	Power/Other	
V_{CC}	T4	Power/Other	
V_{CC}	T6	Power/Other	
V_{CC}	T8	Power/Other	
V_{CC}	T24	Power/Other	
V_{CC}	T26	Power/Other	
V_{CC}	T28	Power/Other	
V_{CC}	T30	Power/Other	
V_{CC}	U23	Power/Other	
V_{CC}	U25	Power/Other	
V_{CC}	U27	Power/Other	
V_{CC}	U29	Power/Other	
V_{CC}	U31	Power/Other	
V_{CC}	V2	Power/Other	
V_{CC}	V4	Power/Other	
V_{CC}	V6	Power/Other	
V_{CC}	V8	Power/Other	
V_{CC}	V24	Power/Other	
V_{CC}	V26	Power/Other	
V_{CC}	V28	Power/Other	
V_{CC}	V30	Power/Other	
V_{CC}	W1	Power/Other	
V_{CC}	W25	Power/Other	
V_{CC}	W27	Power/Other	
V_{CC}	W29	Power/Other	
V_{CC}	W31	Power/Other	
V_{CC}	Y2	Power/Other	
V_{CC}	Y16	Power/Other	
V_{CC}	Y22	Power/Other	
V_{CC}	Y30	Power/Other	
V_{CC}	AA1	Power/Other	
V_{CC}	AA6	Power/Other	
V_{CC}	AA20	Power/Other	
V_{CC}	AA26	Power/Other	
V_{CC}	AA31	Power/Other	
V_{CC}	AB2	Power/Other	

Table 5-1. Pin Listing by Pin Name (cont'd)

Pin Name	Pin No.	Signal Buffer Type	Direction
V_{CC}	AB8	Power/Other	
V_{CC}	AB14	Power/Other	
V_{CC}	AB18	Power/Other	
V_{CC}	AB24	Power/Other	
V_{CC}	AB30	Power/Other	
V_{CC}	AC3	Power/Other	
V_{CC}	AC16	Power/Other	
V_{CC}	AC22	Power/Other	
V_{CC}	AC31	Power/Other	
V_{CC}	AD2	Power/Other	
V_{CC}	AD20	Power/Other	
V_{CC}	AD26	Power/Other	
V_{CC}	AE14	Power/Other	
V_{CC}	AE18	Power/Other	
V_{CC}	AE24	Power/Other	
V_{CCA}	AB4	Power/Other	Input
V_{CCA_CACHE}	AE3	Power/Other	Input
$V_{CC\_CACHE\_SENSE}$	B31	Power/Other	Output
$V_{CCIOPLL}$	AD4	Power/Other	Input
V_{CCPLL}	AD1	Power/Other	Input
$V_{CCSENSE}$	B27	Power/Other	Output
VID0	F3	Power/Other	Output
VID1	E3	Power/Other	Output
VID2	D3	Power/Other	Output
VID3	C3	Power/Other	Output
VID4	B3	Power/Other	Output
VID5	A1	Power/Other	Output
VIDPWRGD	B1	Power/Other	Input
V_{SS}	A5	Power/Other	
V_{SS}	A11	Power/Other	
V_{SS}	A21	Power/Other	
V_{SS}	A27	Power/Other	
V_{SS}	A29	Power/Other	
V_{SS}	B2	Power/Other	
V_{SS}	B9	Power/Other	
V_{SS}	B15	Power/Other	
V_{SS}	B17	Power/Other	

Table 5-1. Pin Listing by Pin Name (cont'd)

Pin Name	Pin No.	Signal Buffer Type	Direction
V_{SS}	B23	Power/Other	
V_{SS}	B28	Power/Other	
V_{SS}	C7	Power/Other	
V_{SS}	C13	Power/Other	
V_{SS}	C19	Power/Other	
V_{SS}	C25	Power/Other	
V_{SS}	C29	Power/Other	
V_{SS}	D2	Power/Other	
V_{SS}	D5	Power/Other	
V_{SS}	D11	Power/Other	
V_{SS}	D21	Power/Other	
V_{SS}	D28	Power/Other	
V_{SS}	D30	Power/Other	
V_{SS}	E9	Power/Other	
V_{SS}	E15	Power/Other	
V_{SS}	E17	Power/Other	
V_{SS}	E23	Power/Other	
V_{SS}	E29	Power/Other	
V_{SS}	E31	Power/Other	
V_{SS}	F2	Power/Other	
V_{SS}	F7	Power/Other	
V_{SS}	F13	Power/Other	
V_{SS}	F19	Power/Other	
V_{SS}	F25	Power/Other	
V_{SS}	F28	Power/Other	
V_{SS}	F30	Power/Other	
V_{SS}	G1	Power/Other	
V_{SS}	G3	Power/Other	
V_{SS}	G5	Power/Other	
V_{SS}	G9	Power/Other	
V_{SS}	G25	Power/Other	
V_{SS}	G27	Power/Other	
V_{SS}	G29	Power/Other	
V_{SS}	G31	Power/Other	
V_{SS}	H2	Power/Other	
V_{SS}	H4	Power/Other	
V_{SS}	H6	Power/Other	

Table 5-1. Pin Listing by Pin Name (cont'd)

Pin Name	Pin No.	Signal Buffer Type	Direction
V_{SS}	H8	Power/Other	
V_{SS}	H24	Power/Other	
V_{SS}	H26	Power/Other	
V_{SS}	H28	Power/Other	
V_{SS}	H30	Power/Other	
V_{SS}	J1	Power/Other	
V_{SS}	J3	Power/Other	
V_{SS}	J5	Power/Other	
V_{SS}	J7	Power/Other	
V_{SS}	J9	Power/Other	
V_{SS}	J23	Power/Other	
V_{SS}	J25	Power/Other	
V_{SS}	J27	Power/Other	
V_{SS}	J29	Power/Other	
V_{SS}	J31	Power/Other	
V_{SS}	K2	Power/Other	
V_{SS}	K4	Power/Other	
V_{SS}	K6	Power/Other	
V_{SS}	K8	Power/Other	
V_{SS}	K24	Power/Other	
V_{SS}	K26	Power/Other	
V_{SS}	K28	Power/Other	
V_{SS}	K30	Power/Other	
V_{SS}	L1	Power/Other	
V_{SS}	L3	Power/Other	
V_{SS}	L5	Power/Other	
V_{SS}	L7	Power/Other	
V_{SS}	L9	Power/Other	
V_{SS}	L23	Power/Other	
V_{SS}	L25	Power/Other	
V_{SS}	L27	Power/Other	
V_{SS}	L29	Power/Other	
V_{SS}	L31	Power/Other	
V_{SS}	M2	Power/Other	
V_{SS}	M4	Power/Other	
V_{SS}	M6	Power/Other	
V_{SS}	M8	Power/Other	

Table 5-1. Pin Listing by Pin Name (cont'd)

Pin Name	Pin No.	Signal Buffer Type	Direction
V_{SS}	M24	Power/Other	
V_{SS}	M26	Power/Other	
V_{SS}	M28	Power/Other	
V_{SS}	M30	Power/Other	
V_{SS}	N2	Power/Other	
V_{SS}	N4	Power/Other	
V_{SS}	N6	Power/Other	
V_{SS}	N8	Power/Other	
V_{SS}	N24	Power/Other	
V_{SS}	N26	Power/Other	
V_{SS}	N28	Power/Other	
V_{SS}	N30	Power/Other	
V_{SS}	P1	Power/Other	
V_{SS}	P3	Power/Other	
V_{SS}	P5	Power/Other	
V_{SS}	P7	Power/Other	
V_{SS}	P9	Power/Other	
V_{SS}	P23	Power/Other	
V_{SS}	P25	Power/Other	
V_{SS}	P27	Power/Other	
V_{SS}	P29	Power/Other	
V_{SS}	P31	Power/Other	
V_{SS}	R2	Power/Other	
V_{SS}	R4	Power/Other	
V_{SS}	R6	Power/Other	
V_{SS}	R8	Power/Other	
V_{SS}	R24	Power/Other	
V_{SS}	R26	Power/Other	
V_{SS}	R28	Power/Other	
V_{SS}	R30	Power/Other	
V_{SS}	T1	Power/Other	
V_{SS}	T3	Power/Other	
V_{SS}	T5	Power/Other	
V_{SS}	T7	Power/Other	
V_{SS}	T9	Power/Other	
V_{SS}	T23	Power/Other	
V_{SS}	T25	Power/Other	

Table 5-1. Pin Listing by Pin Name (cont'd)

Pin Name	Pin No.	Signal Buffer Type	Direction
V_{SS}	T27	Power/Other	
V_{SS}	T29	Power/Other	
V_{SS}	T31	Power/Other	
V_{SS}	U2	Power/Other	
V_{SS}	U4	Power/Other	
V_{SS}	U6	Power/Other	
V_{SS}	U8	Power/Other	
V_{SS}	U24	Power/Other	
V_{SS}	U26	Power/Other	
V_{SS}	U28	Power/Other	
V_{SS}	U30	Power/Other	
V_{SS}	V1	Power/Other	
V_{SS}	V3	Power/Other	
V_{SS}	V5	Power/Other	
V_{SS}	V7	Power/Other	
V_{SS}	V9	Power/Other	
V_{SS}	V23	Power/Other	
V_{SS}	V25	Power/Other	
V_{SS}	V27	Power/Other	
V_{SS}	V29	Power/Other	
V_{SS}	V31	Power/Other	
V_{SS}	W2	Power/Other	
V_{SS}	W4	Power/Other	
V_{SS}	W24	Power/Other	
V_{SS}	W26	Power/Other	
V_{SS}	W28	Power/Other	
V_{SS}	W30	Power/Other	
V_{SS}	Y1	Power/Other	
V_{SS}	Y3	Power/Other	
V_{SS}	Y5	Power/Other	
V_{SS}	Y7	Power/Other	
V_{SS}	Y13	Power/Other	
V_{SS}	Y19	Power/Other	
V_{SS}	Y25	Power/Other	
V_{SS}	Y31	Power/Other	
V_{SS}	AA2	Power/Other	
V_{SS}	AA9	Power/Other	

Table 5-1. Pin Listing by Pin Name (cont'd)

Pin Name	Pin No.	Signal Buffer Type	Direction
V_{SS}	AA15	Power/Other	
V_{SS}	AA17	Power/Other	
V_{SS}	AA23	Power/Other	
V_{SS}	AA30	Power/Other	
V_{SS}	AB1	Power/Other	
V_{SS}	AB5	Power/Other	
V_{SS}	AB11	Power/Other	
V_{SS}	AB21	Power/Other	
V_{SS}	AB27	Power/Other	
V_{SS}	AB31	Power/Other	
V_{SS}	AC2	Power/Other	
V_{SS}	AC7	Power/Other	
V_{SS}	AC13	Power/Other	
V_{SS}	AC19	Power/Other	
V_{SS}	AC25	Power/Other	
V_{SS}	AD3	Power/Other	
V_{SS}	AD9	Power/Other	
V_{SS}	AD15	Power/Other	
V_{SS}	AD17	Power/Other	
V_{SS}	AD23	Power/Other	
V_{SS}	AE6	Power/Other	
V_{SS}	AE11	Power/Other	
V_{SS}	AE21	Power/Other	
V_{SS}	AE27	Power/Other	

Table 5-1. Pin Listing by Pin Name (cont'd)

Pin Name	Pin No.	Signal Buffer Type	Direction
V_{SSA}	AA5	Power/Other	Input
V_{SSA_CACHE}	AE2	Power/Other	Input
$V_{SS\_CACHE\_SENSE}$	C31	Power/Other	Output
$V_{SSSENSE}$	D26	Power/Other	Output
V_{TT}	A4	Power/Other	
V_{TT}	B12	Power/Other	
V_{TT}	C5	Power/Other	
V_{TT}	C10	Power/Other	
V_{TT}	E12	Power/Other	
V_{TT}	F10	Power/Other	
V_{TT}	Y10	Power/Other	
V_{TT}	AA12	Power/Other	
V_{TT}	AC10	Power/Other	
V_{TT}	AD12	Power/Other	
VTTEN	E1	Power/Other	Output

NOTES:
1. In systems utilizing the 64-bit Intel® Xeon™ processor MP with up to 8MB L3 cache, the system designer must pull-up these signals to the processor V_{TT}.

5.1.2 Pin Listing by Pin Number

Table 5-2. Pin Listing by Pin Number

Pin No.	Pin Name	Signal Buffer Type	Direction
A1	VID5	Power/Other	Output
A2	CVID3	Power/Other	Output
A3	SKTOCC#	Power/Other	Output
A4	V_{TT}	Power/Other	
A5	V_{SS}	Power/Other	
A6	A32#	Source Sync	Input/Output
A7	A33#	Source Sync	Input/Output
A8	V_{CC}	Power/Other	
A9	A26#	Source Sync	Input/Output
A10	A20#	Source Sync	Input/Output
A11	V_{SS}	Power/Other	
A12	A14#	Source Sync	Input/Output
A13	A10#	Source Sync	Input/Output
A14	V_{CC}	Power/Other	
A15	FORCEPR#	Power/Other	Input
A16	TEST_BUS	Power/Other	Input
A17	LOCK#	Common Clk	Input/Output
A18	V_{CC}	Power/Other	
A19	A7#	Source Sync	Input/Output
A20	A4#	Source Sync	Input/Output
A21	V_{SS}	Power/Other	
A22	A3#	Source Sync	Input/Output
A23	HITM#	Common Clk	Input/Output
A24	V_{CC}	Power/Other	
A25	TMS	TAP	Input
A26	ID0#	Common Clk	Input
A27	V_{SS}	Power/Other	
A28	IDS#	Common Clk	Input
A29	V_{SS}	Power/Other	
A30	ID7#	Common Clk	Input
A31	Reserved		
B1	VIDPWRGD	Power/Other	Input

Table 5-2. Pin Listing by Pin Number (cont'd)

Pin No.	Pin Name	Signal Buffer Type	Direction
B2	V_{SS}	Power/Other	
B3	VID4	Power/Other	Output
B4	V_{CACHE}	Power/Other	
B5	ODTEN	Power/Other	Input
B6	A38#	Source Sync	Input/Output
B7	A31#	Source Sync	Input/Output
B8	A27#	Source Sync	Input/Output
B9	V_{SS}	Power/Other	
B10	A21#	Source Sync	Input/Output
B11	A22#	Source Sync	Input/Output
B12	V_{TT}	Power/Other	
B13	A13#	Source Sync	Input/Output
B14	A12#	Source Sync	Input/Output
B15	V_{SS}	Power/Other	
B16	A11#	Source Sync	Input/Output
B17	V_{SS}	Power/Other	
B18	A5#	Source Sync	Input/Output
B19	REQ0#	Common Clk	Input/Output
B20	V_{CC}	Power/Other	
B21	REQ1#	Common Clk	Input/Output
B22	REQ4#	Common Clk	Input/Output
B23	V_{SS}	Power/Other	
B24	LINT0/INTR	Async GTL+	Input
B25	PROCHOT#	Power/Other	Output
B26	ID1#	Common Clk	Input
B27	$V_{CCSENSE}$	Power/Other	Output
B28	V_{SS}	Power/Other	
B29	ID5#	Common Clk	Input
B30	ID6#	Common Clk	Input
B31	$V_{CC\_CACHE\_SENSE}$	Power/Other	
C1	Reserved		
C2	CVID2	Power/Other	Output

Table 5-2. Pin Listing by Pin Number (cont'd)

Pin No.	Pin Name	Signal Buffer Type	Direction
C3	VID3	Power/Other	Output
C4	V_{CC}	Power/Other	
C5	V_{TT}	Power/Other	
C6	RSP#	Common Clk	Input
C7	V_{SS}	Power/Other	
C8	A35#	Source Sync	Input/Output
C9	A34#	Source Sync	Input/Output
C10	V_{TT}	Power/Other	
C11	A30#	Source Sync	Input/Output
C12	A23#	Source Sync	Input/Output
C13	V_{SS}	Power/Other	
C14	A16#	Source Sync	Input/Output
C15	A15#	Source Sync	Input/Output
C16	A39#	Source Sync	Input/Output
C17	A8#	Source Sync	Input/Output
C18	A6#	Source Sync	Input/Output
C19	V_{SS}	Power/Other	
C20	REQ3#	Common Clk	Input/Output
C21	REQ2#	Common Clk	Input/Output
C22	V_{CC}	Power/Other	
C23	DEFER#	Common Clk	Input
C24	TDI	TAP	Input
C25	V_{SS}	Power/Other	Input
C26	IGNNE#	Async GTL+	Input
C27	SMI#	Async GTL+	Input
C28	ID4#	Common Clk	Input
C29	V_{SS}	Power/Other	
C30	V_{CC}	Power/Other	
C31	$V_{SS\_CACHE\_SENSE}$	Power/Other	
D1	CVID1	Power/Other	Output
D2	V_{SS}	Power/Other	
D3	VID2	Power/Other	Output
D4	STPCLK#	Async GTL+	Input
D5	V_{SS}	Power/Other	
D6	INIT#	Async GTL+	Input

Table 5-2. Pin Listing by Pin Number (cont'd)

Pin No.	Pin Name	Signal Buffer Type	Direction
D7	MCERR#	Common Clk	Input/Output
D8	V_{CC}	Power/Other	
D9	AP1#	Common Clk	Input/Output
D10	BR3#[1]	Common Clk	Input
D11	V_{SS}	Power/Other	
D12	A29#	Source Sync	Input/Output
D13	A25#	Source Sync	Input/Output
D14	V_{CC}	Power/Other	
D15	A18#	Source Sync	Input/Output
D16	A17#	Source Sync	Input/Output
D17	A9#	Source Sync	Input/Output
D18	V_{CC}	Power/Other	
D19	ADS#	Common Clk	Input/Output
D20	BR0#	Common Clk	Input/Output
D21	V_{SS}	Power/Other	
D22	RS1#	Common Clk	Input
D23	BPRI#	Common Clk	Input
D24	V_{CC}	Power/Other	
D25	ID2#	Common Clk	Input
D26	$V_{SSSENSE}$	Power/Other	Output
D27	ID3#	Common Clk	Input
D28	V_{SS}	Power/Other	
D29	OOD#	Common Clk	Input
D30	V_{SS}	Power/Other	
D31	V_{CC}	Power/Other	
E1	VTTEN	Power/Other	Output
E2	CVID0	Power/Other	Output
E3	VID1	Power/Other	Output
E4	BPM5#	Common Clk	Input/Output
E5	IERR#	Common Clk	Output

Table 5-2. Pin Listing by Pin Number (cont'd)

Pin No.	Pin Name	Signal Buffer Type	Direction
E6	V_{CC}	Power/Other	
E7	BPM2#	Common Clk	Input/Output
E8	BPM4#	Common Clk	Input/Output
E9	V_{SS}	Power/Other	
E10	AP0#	Common Clk	Input/Output
E11	BR2#[1]	Common Clk	Input
E12	V_{TT}	Power/Other	
E13	A28#	Source Sync	Input/Output
E14	A24#	Source Sync	Input/Output
E15	V_{SS}	Power/Other	
E16	Reserved		
E17	V_{SS}	Power/Other	
E18	DRDY#	Common Clk	Input/Output
E19	TRDY#	Common Clk	Input
E20	V_{CC}	Power/Other	
E21	RS0#	Common Clk	Input
E22	HIT#	Common Clk	Input/Output
E23	V_{SS}	Power/Other	
E24	TCK	TAP	Input
E25	TDO	TAP	Output
E26	V_{CC}	Power/Other	
E27	FERR#/PBE#	Async GTL+	Output
E28	V_{CC}	Power/Other	
E29	V_{SS}	Power/Other	
E30	V_{CC}	Power/Other	
E31	V_{SS}	Power/Other	
F1	V_{CC}	Power/Other	
F2	V_{SS}	Power/Other	
F3	VID0	Power/Other	Output
F4	V_{CC}	Power/Other	
F5	BPM3#	Common Clk	Input/Output

Table 5-2. Pin Listing by Pin Number (cont'd)

Pin No.	Pin Name	Signal Buffer Type	Direction
F6	BPM0#	Common Clk	Input/Output
F7	V_{SS}	Power/Other	
F8	BPM1#	Common Clk	Input/Output
F9	GTLREF3	Power/Other	Input
F10	V_{TT}	Power/Other	
F11	BINIT#	Common Clk	Input/Output
F12	BR1#	Common Clk	Input
F13	V_{SS}	Power/Other	
F14	ADSTB1#	Source Sync	Input/Output
F15	A19#	Source Sync	Input/Output
F16	A36#	Source Sync	Input/Output
F17	ADSTB0#	Source Sync	Input/Output
F18	DBSY#	Common Clk	Input/Output
F19	V_{SS}	Power/Other	
F20	BNR#	Common Clk	Input/Output
F21	RS2#	Common Clk	Input
F22	A37#	Source Sync	Input/Output
F23	GTLREF2	Power/Other	Input
F24	TRST#	TAP	Input
F25	V_{SS}	Power/Other	
F26	THERMTRIP#	Async GTL+	Output
F27	A20M#	Async GTL+	Input
F28	V_{SS}	Power/Other	
F29	V_{CC}	Power/Other	
F30	V_{SS}	Power/Other	
F31	V_{CC}	Power/Other	
G1	V_{SS}	Power/Other	
G2	V_{CC}	Power/Other	
G3	V_{SS}	Power/Other	
G4	V_{CC}	Power/Other	
G5	V_{SS}	Power/Other	
G6	V_{CC}	Power/Other	
G7	BOOT_SELECT	Power/Other	Input

Table 5-2. Pin Listing by Pin Number (cont'd)

Pin No.	Pin Name	Signal Buffer Type	Direction
G8	V_{CC}	Power/Other	
G9	V_{SS}	Power/Other	
G23	LINT1/NMI	Async GTL+	Input
G24	V_{CC}	Power/Other	
G25	V_{SS}	Power/Other	
G26	V_{CC}	Power/Other	
G27	V_{SS}	Power/Other	
G28	V_{CC}	Power/Other	
G29	V_{SS}	Power/Other	
G30	V_{CC}	Power/Other	
G31	V_{SS}	Power/Other	
H1	V_{CACHE}	Power/Other	
H2	V_{SS}	Power/Other	
H3	V_{CACHE}	Power/Other	
H4	V_{SS}	Power/Other	
H5	V_{CACHE}	Power/Other	
H6	V_{SS}	Power/Other	
H7	V_{CACHE}	Power/Other	
H8	V_{SS}	Power/Other	
H9	V_{CACHE}	Power/Other	
H23	V_{CC}	Power/Other	
H24	V_{SS}	Power/Other	
H25	V_{CC}	Power/Other	
H26	V_{SS}	Power/Other	
H27	V_{CC}	Power/Other	
H28	V_{SS}	Power/Other	
H29	V_{CC}	Power/Other	
H30	V_{SS}	Power/Other	
H31	V_{CC}	Power/Other	
J1	V_{SS}	Power/Other	
J2	V_{CC}	Power/Other	
J3	V_{SS}	Power/Other	
J4	V_{CC}	Power/Other	
J5	V_{SS}	Power/Other	
J6	V_{CC}	Power/Other	
J7	V_{SS}	Power/Other	
J8	V_{CC}	Power/Other	

Table 5-2. Pin Listing by Pin Number (cont'd)

Pin No.	Pin Name	Signal Buffer Type	Direction
J9	V_{SS}	Power/Other	
J23	V_{SS}	Power/Other	
J24	V_{CC}	Power/Other	
J25	V_{SS}	Power/Other	
J26	V_{CC}	Power/Other	
J27	V_{SS}	Power/Other	
J28	V_{CC}	Power/Other	
J29	V_{SS}	Power/Other	
J30	V_{CC}	Power/Other	
J31	V_{SS}	Power/Other	
K1	V_{CACHE}	Power/Other	
K2	V_{SS}	Power/Other	
K3	V_{CACHE}	Power/Other	
K4	V_{SS}	Power/Other	
K5	V_{CACHE}	Power/Other	
K6	V_{SS}	Power/Other	
K7	V_{CACHE}	Power/Other	
K8	V_{SS}	Power/Other	
K9	V_{CACHE}	Power/Other	
K23	V_{CC}	Power/Other	
K24	V_{SS}	Power/Other	
K25	V_{CC}	Power/Other	
K26	V_{SS}	Power/Other	
K27	V_{CC}	Power/Other	
K28	V_{SS}	Power/Other	
K29	V_{CC}	Power/Other	
K30	V_{SS}	Power/Other	
K31	V_{CC}	Power/Other	
L1	V_{SS}	Power/Other	
L2	V_{CC}	Power/Other	
L3	V_{SS}	Power/Other	
L4	V_{CC}	Power/Other	
L5	V_{SS}	Power/Other	
L6	V_{CC}	Power/Other	
L7	V_{SS}	Power/Other	
L8	V_{CC}	Power/Other	
L9	V_{SS}	Power/Other	

Table 5-2. Pin Listing by Pin Number (cont'd)

Pin No.	Pin Name	Signal Buffer Type	Direction
L23	V_{SS}	Power/Other	
L24	V_{CC}	Power/Other	
L25	V_{SS}	Power/Other	
L26	V_{CC}	Power/Other	
L27	V_{SS}	Power/Other	
L28	V_{CC}	Power/Other	
L29	V_{SS}	Power/Other	
L30	V_{CC}	Power/Other	
L31	V_{SS}	Power/Other	
M1	V_{CACHE}	Power/Other	
M2	V_{SS}	Power/Other	
M3	V_{CACHE}	Power/Other	
M4	V_{SS}	Power/Other	
M5	V_{CACHE}	Power/Other	
M6	V_{SS}	Power/Other	
M7	V_{CACHE}	Power/Other	
M8	V_{SS}	Power/Other	
M9	V_{CACHE}	Power/Other	
M23	V_{CC}	Power/Other	
M24	V_{SS}	Power/Other	
M25	V_{CC}	Power/Other	
M26	V_{SS}	Power/Other	
M27	V_{CC}	Power/Other	
M28	V_{SS}	Power/Other	
M29	V_{CC}	Power/Other	
M30	V_{SS}	Power/Other	
M31	V_{CC}	Power/Other	
N1	V_{CACHE}	Power/Other	
N2	V_{SS}	Power/Other	
N3	V_{CACHE}	Power/Other	
N4	V_{SS}	Power/Other	
N5	V_{CACHE}	Power/Other	
N6	V_{SS}	Power/Other	
N7	V_{CACHE}	Power/Other	
N8	V_{SS}	Power/Other	
N9	V_{CACHE}	Power/Other	
N23	V_{CC}	Power/Other	

Table 5-2. Pin Listing by Pin Number (cont'd)

Pin No.	Pin Name	Signal Buffer Type	Direction
N24	V_{SS}	Power/Other	
N25	V_{CC}	Power/Other	
N26	V_{SS}	Power/Other	
N27	V_{CC}	Power/Other	
N28	V_{SS}	Power/Other	
N29	V_{CC}	Power/Other	
N30	V_{SS}	Power/Other	
N31	V_{CC}	Power/Other	
P1	V_{SS}	Power/Other	
P2	V_{CC}	Power/Other	
P3	V_{SS}	Power/Other	
P4	V_{CC}	Power/Other	
P5	V_{SS}	Power/Other	
P6	V_{CC}	Power/Other	
P7	V_{SS}	Power/Other	
P8	V_{CC}	Power/Other	
P9	V_{SS}	Power/Other	
P23	V_{SS}	Power/Other	
P24	V_{CC}	Power/Other	
P25	V_{SS}	Power/Other	
P26	V_{CC}	Power/Other	
P27	V_{SS}	Power/Other	
P28	V_{CC}	Power/Other	
P29	V_{SS}	Power/Other	
P30	V_{CC}	Power/Other	
P31	V_{SS}	Power/Other	
R1	V_{CACHE}	Power/Other	
R2	V_{SS}	Power/Other	
R3	V_{CACHE}	Power/Other	
R4	V_{SS}	Power/Other	
R5	V_{CACHE}	Power/Other	
R6	V_{SS}	Power/Other	
R7	V_{CACHE}	Power/Other	
R8	V_{SS}	Power/Other	
R9	V_{CACHE}	Power/Other	
R23	V_{CC}	Power/Other	
R24	V_{SS}	Power/Other	

Table 5-2. Pin Listing by Pin Number (cont'd)

Pin No.	Pin Name	Signal Buffer Type	Direction
R25	V_{CC}	Power/Other	
R26	V_{SS}	Power/Other	
R27	V_{CC}	Power/Other	
R28	V_{SS}	Power/Other	
R29	V_{CC}	Power/Other	
R30	V_{SS}	Power/Other	
R31	V_{CC}	Power/Other	
T1	V_{SS}	Power/Other	
T2	V_{CC}	Power/Other	
T3	V_{SS}	Power/Other	
T4	V_{CC}	Power/Other	
T5	V_{SS}	Power/Other	
T6	V_{CC}	Power/Other	
T7	V_{SS}	Power/Other	
T8	V_{CC}	Power/Other	
T9	V_{SS}	Power/Other	
T23	V_{SS}	Power/Other	
T24	V_{CC}	Power/Other	
T25	V_{SS}	Power/Other	
T26	V_{CC}	Power/Other	
T27	V_{SS}	Power/Other	
T28	V_{CC}	Power/Other	
T29	V_{SS}	Power/Other	
T30	V_{CC}	Power/Other	
T31	V_{SS}	Power/Other	
U1	V_{CACHE}	Power/Other	
U2	V_{SS}	Power/Other	
U3	V_{CACHE}	Power/Other	
U4	V_{SS}	Power/Other	
U5	V_{CACHE}	Power/Other	
U6	V_{SS}	Power/Other	
U7	V_{CACHE}	Power/Other	
U8	V_{SS}	Power/Other	
U9	V_{CACHE}	Power/Other	
U23	V_{CC}	Power/Other	
U24	V_{SS}	Power/Other	
U25	V_{CC}	Power/Other	

Table 5-2. Pin Listing by Pin Number (cont'd)

Pin No.	Pin Name	Signal Buffer Type	Direction
U26	V_{SS}	Power/Other	
U27	V_{CC}	Power/Other	
U28	V_{SS}	Power/Other	
U29	V_{CC}	Power/Other	
U30	V_{SS}	Power/Other	
U31	V_{CC}	Power/Other	
V1	V_{SS}	Power/Other	
V2	V_{CC}	Power/Other	
V3	V_{SS}	Power/Other	
V4	V_{CC}	Power/Other	
V5	V_{SS}	Power/Other	
V6	V_{CC}	Power/Other	
V7	V_{SS}	Power/Other	
V8	V_{CC}	Power/Other	
V9	V_{SS}	Power/Other	
V23	V_{SS}	Power/Other	
V24	V_{CC}	Power/Other	
V25	V_{SS}	Power/Other	
V26	V_{CC}	Power/Other	
V27	V_{SS}	Power/Other	
V28	V_{CC}	Power/Other	
V29	V_{SS}	Power/Other	
V30	V_{CC}	Power/Other	
V31	V_{SS}	Power/Other	
W1	V_{CC}	Power/Other	
W2	V_{SS}	Power/Other	
W3	Reserved		
W4	V_{SS}	Power/Other	
W5	BCLK1	FSB Clk	Input
W6	TESTHI0	Power/Other	Input
W7	TESTHI1	Power/Other	Input
W8	TESTHI2	Power/Other	Input
W9	GTLREF1	Power/Other	Input
W23	GTLREF0	Power/Other	Input
W24	V_{SS}	Power/Other	
W25	V_{CC}	Power/Other	
W26	V_{SS}	Power/Other	

Table 5-2. Pin Listing by Pin Number (cont'd)

Pin No.	Pin Name	Signal Buffer Type	Direction
W27	V_{CC}	Power/Other	
W28	V_{SS}	Power/Other	
W29	V_{CC}	Power/Other	
W30	V_{SS}	Power/Other	
W31	V_{CC}	Power/Other	
Y1	V_{SS}	Power/Other	
Y2	V_{CC}	Power/Other	
Y3	V_{SS}	Power/Other	
Y4	BCLK0	FSB Clk	Input
Y5	V_{SS}	Power/Other	
Y6	TESTHI3	Power/Other	Input
Y7	V_{SS}	Power/Other	
Y8	RESET#	Common Clk	Input
Y9	D62#	Source Sync	Input/Output
Y10	V_{TT}	Power/Other	
Y11	DSTBP3#	Source Sync	Input/Output
Y12	DSTBN3#	Source Sync	Input/Output
Y13	V_{SS}	Power/Other	
Y14	DSTBP2#	Source Sync	Input/Output
Y15	DSTBN2#	Source Sync	Input/Output
Y16	V_{CC}	Power/Other	
Y17	DSTBP1#	Source Sync	Input/Output
Y18	DSTBN1#	Source Sync	Input/Output
Y19	V_{SS}	Power/Other	
Y20	DSTBP0#	Source Sync	Input/Output
Y21	DSTBN0#	Source Sync	Input/Output
Y22	V_{CC}	Power/Other	
Y23	D5#	Source Sync	Input/Output
Y24	D2#	Source Sync	Input/Output
Y25	V_{SS}	Power/Other	
Y26	D0#	Source Sync	Input/Output
Y27	Reserved		
Y28	Reserved		
Y29	SM_TS1_A1	SMBus	Input
Y30	V_{CC}	Power/Other	
Y31	V_{SS}	Power/Other	

Table 5-2. Pin Listing by Pin Number (cont'd)

Pin No.	Pin Name	Signal Buffer Type	Direction
AA1	V_{CC}	Power/Other	
AA2	V_{SS}	Power/Other	
AA3	BSEL0	Power/Other	Output
AA4	DEP7#	Source Sync	Input/Output
AA5	V_{SSA}	Power/Other	Input
AA6	V_{CC}	Power/Other	
AA7	TESTHI4	Power/Other	Input
AA8	D61#	Source Sync	Input/Output
AA9	V_{SS}	Power/Other	
AA10	D54#	Source Sync	Input/Output
AA11	D53#	Source Sync	Input/Output
AA12	V_{TT}	Power/Other	
AA13	D48#	Source Sync	Input/Output
AA14	D49#	Source Sync	Input/Output
AA15	V_{SS}	Power/Other	
AA16	D33#	Source Sync	Input/Output
AA17	V_{SS}	Power/Other	
AA18	D24#	Source Sync	Input/Output
AA19	D15#	Source Sync	Input/Output
AA20	V_{CC}	Power/Other	
AA21	D11#	Source Sync	Input/Output
AA22	D10#	Source Sync	Input/Output
AA23	V_{SS}	Power/Other	
AA24	D6#	Source Sync	Input/Output
AA25	D3#	Source Sync	Input/Output
AA26	V_{CC}	Power/Other	
AA27	D1#	Source Sync	Input/Output
AA28	SM_TS1_A0	SMBus	Input
AA29	SM_EP_A0	SMBus	Input
AA30	V_{SS}	Power/Other	
AA31	V_{CC}	Power/Other	
AB1	V_{SS}	Power/Other	
AB2	V_{CC}	Power/Other	
AB3	BSEL1	Power/Other	Output
AB4	V_{CCA}	Power/Other	Input
AB5	V_{SS}	Power/Other	
AB6	D63#	Source Sync	Input/Output

Table 5-2. Pin Listing by Pin Number (cont'd)

Pin No.	Pin Name	Signal Buffer Type	Direction
AB7	PWRGOOD	Async GTL+	Input
AB8	V_{CC}	Power/Other	
AB9	DBI3#	Source Sync	Input/Output
AB10	D55#	Source Sync	Input/Output
AB11	V_{SS}	Power/Other	
AB12	D51#	Source Sync	Input/Output
AB13	D52#	Source Sync	Input/Output
AB14	V_{CC}	Power/Other	
AB15	D37#	Source Sync	Input/Output
AB16	D32#	Source Sync	Input/Output
AB17	D31#	Source Sync	Input/Output
AB18	V_{CC}	Power/Other	
AB19	D14#	Source Sync	Input/Output
AB20	D12#	Source Sync	Input/Output
AB21	V_{SS}	Power/Other	
AB22	D13#	Source Sync	Input/Output
AB23	D9#	Source Sync	Input/Output
AB24	V_{CC}	Power/Other	
AB25	D8#	Source Sync	Input/Output
AB26	D7#	Source Sync	Input/Output
AB27	V_{SS}	Power/Other	
AB28	SM_EP_A2	SMBus	Input
AB29	SM_EP_A1	SMBus	Input
AB30	V_{CC}	Power/Other	
AB31	V_{SS}	Power/Other	
AC1	Reserved		
AC2	V_{SS}	Power/Other	
AC3	V_{CC}	Power/Other	
AC4	DEP6#	Source Sync	Input/Output
AC5	D60#	Source Sync	Input/Output
AC6	D59#	Source Sync	Input/Output
AC7	V_{SS}	Power/Other	
AC8	D56#	Source Sync	Input/Output
AC9	D47#	Source Sync	Input/Output
AC10	V_{TT}	Power/Other	
AC11	D43#	Source Sync	Input/Output
AC12	D41#	Source Sync	Input/Output

Table 5-2. Pin Listing by Pin Number (cont'd)

Pin No.	Pin Name	Signal Buffer Type	Direction
AC13	V_{SS}	Power/Other	
AC14	D50#	Source Sync	Input/Output
AC15	DP2#	Common Clk	Input/Output
AC16	V_{CC}	Power/Other	
AC17	D34#	Source Sync	Input/Output
AC18	DP0#	Common Clk	Input/Output
AC19	V_{SS}	Power/Other	
AC20	D25#	Source Sync	Input/Output
AC21	D26#	Source Sync	Input/Output
AC22	V_{CC}	Power/Other	
AC23	D23#	Source Sync	Input/Output
AC24	D20#	Source Sync	Input/Output
AC25	V_{SS}	Power/Other	
AC26	D17#	Source Sync	Input/Output
AC27	DBI0#	Source Sync	Input/Output
AC28	SM_CLK	SMBus	Input
AC29	SM_DAT	SMBus	Output
AC30	SLEW_CTRL	Power/Other	Input
AC31	V_{CC}	Power/Other	
AD1	V_{CCPLL}	Power/Other	Input
AD2	V_{CC}	Power/Other	
AD3	V_{SS}	Power/Other	
AD4	$V_{CCIOPLL}$	Power/Other	Input
AD5	TESTHI5	Power/Other	Input
AD6	DEP5#	Source Sync	Input/Output
AD7	D57#	Source Sync	Input/Output
AD8	D46#	Source Sync	Input/Output
AD9	V_{SS}	Power/Other	
AD10	D45#	Source Sync	Input/Output
AD11	D40#	Source Sync	Input/Output
AD12	V_{TT}	Power/Other	
AD13	D38#	Source Sync	Input/Output
AD14	D39#	Source Sync	Input/Output
AD15	V_{SS}	Power/Other	
AD16	COMP0	Power/Other	Input
AD17	V_{SS}	Power/Other	

Table 5-2. Pin Listing by Pin Number (cont'd)

Pin No.	Pin Name	Signal Buffer Type	Direction
AD18	D36#	Source Sync	Input/Output
AD19	D30#	Source Sync	Input/Output
AD20	V_{CC}	Power/Other	
AD21	D29#	Source Sync	Input/Output
AD22	DBI1#	Source Sync	Input/Output
AD23	V_{SS}	Power/Other	
AD24	D21#	Source Sync	Input/Output
AD25	D18#	Source Sync	Input/Output
AD26	V_{CC}	Power/Other	
AD27	D4#	Source Sync	Input/Output
AD28	SM_ALERT#	SMBus	Output
AD29	SM_WP	SMBus	Input
AD30	DEP1#	Source Sync	Input/Output
AD31	DEP0#	Source Sync	Input/Output
AE2	V_{SSA_CACHE}	Power/Other	Input
AE3	V_{CCA_CACHE}	Power/Other	Input
AE4	Reserved		
AE5	TESTHI6	Power/Other	Input
AE6	V_{SS}	Power/Other	
AE7	D58#	Source Sync	Input/Output
AE8	DEP4#	Source Sync	Input/Output
AE9	D44#	Source Sync	Input/Output
AE10	D42#	Source Sync	Input/Output
AE11	V_{SS}	Power/Other	

Table 5-2. Pin Listing by Pin Number (cont'd)

Pin No.	Pin Name	Signal Buffer Type	Direction
AE12	DBI2#	Source Sync	Input/Output
AE13	D35#	Source Sync	Input/Output
AE14	V_{CC}	Power/Other	
AE15	DEP3#	Source Sync	Input/Output
AE16	DEP2#	Source Sync	Input/Output
AE17	DP3#	Common Clk	Input/Output
AE18	V_{CC}	Power/Other	
AE19	DP1#	Common Clk	Input/Output
AE20	D28#	Source Sync	Input/Output
AE21	V_{SS}	Power/Other	
AE22	D27#	Source Sync	Input/Output
AE23	D22#	Source Sync	Input/Output
AE24	V_{CC}	Power/Other	
AE25	D19#	Source Sync	Input/Output
AE26	D16#	Source Sync	Input/Output
AE27	V_{SS}	Power/Other	
AE28	SM_VCC	Power/Other	
AE29	SM_VCC	Power/Other	
AE30	Reserved		

NOTES:
1. In systems utilizing the 64-bit Intel® Xeon™ processor MP with up to 8MB L3 cache, the system designer must pull-up these signals to the processor V_{TT}.

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6 Signal Definitions

6.1 Signal Definitions

Table 6-1. Signal Definitions (Sheet 1 of 9)

Name	Type	Description
A[39:3]#	I/O	A[39:3]# (Address) define a 2^{40}-byte physical memory address space. In sub-phase 1 of the address phase, these pins transmit the address of a transaction. In sub-phase 2, these pins transmit transaction type information. These signals must connect the appropriate pins of all agents on the processor front side bus. A[39:3]# are protected by parity signals AP[1:0]#. A[39:3]# are source synchronous signals and are latched into the receiving buffers by ADSTB[1:0]#. On the active-to-inactive transition of RESET#, the processors sample a subset of the A[39:3]# pins to determine their power-on configuration. See Section 8.1.
A20M#	I	If A20M# (Address-20 Mask) is asserted, the processor masks physical address bit 20 (A20#) before looking up a line in any internal cache and before driving a read/write transaction on the bus. Asserting A20M# emulates the 8086 processor's address wrap-around at the 1-Mbyte boundary. Assertion of A20M# is only supported in real mode. A20M# is an asynchronous signal. However, to ensure recognition of this signal following an I/O write instruction, it must be valid 6 clks before the I/O write's response.
ADS#	I/O	ADS# (Address Strobe) is asserted to indicate the validity of the transaction address on the A[39:3]# and transaction request type on REQ[4:0]# pins. All bus agents observe the ADS# activation to begin parity checking, protocol checking, address decode, internal snoop, or deferred reply ID match operations associated with the new transaction. This signal must connect the appropriate pins on all processor front side bus agents.
ADSTB[1:0]#	I/O	Address strobes are used to latch A[39:3]# and REQ[4:0]# on their rising and falling edge.
AP[1:0]#	I/O	AP[1:0]# (Address Parity) are driven by the requestor one common clock after ADS#, A[39:3]#, REQ[4:0]# are driven. A correct parity signal is electrically high if an even number of covered signals are electrically low and electrically low if an odd number of covered signals are electrically low. This allows parity to be electrically high when all the covered signals are electrically high. AP[1:0]# should connect the appropriate pins of all processor front side bus agents. The following table defines the coverage for these signals. **Request Signals / Subphase 1 / Subphase 2** A[39:24]# / AP0# / AP1# A[23:3]# / AP1# / AP0# REQ[4:0]# / AP1# / AP0#
BCLK[1:0]	I	The differential bus clock pair BCLK[1:0] determines the bus frequency. All processor front side bus agents must receive these signals to drive their outputs and latch their inputs. All external timing parameters are specified with respect to the rising edge of BCLK0 crossing the falling edge of BCLK1.

Table 6-1. Signal Definitions (Sheet 2 of 9)

Name	Type	Description
BINIT#	I/O	BINIT# (Bus Initialization) may be observed and driven by all processor front side bus agents. If used, BINIT# must connect the appropriate pins of all such agents. If the BINIT# driver is enabled, BINIT# is asserted to signal any bus condition that prevents reliable future operation. If BINIT# observation is enabled during power-on configuration (see Section 8.1) and BINIT# is sampled asserted, symmetric agents reset their bus LOCK# activity and bus request arbitration state machines. The bus agents **do not** reset their I/O Queue (IOQ) and transaction tracking state machines upon observation of BINIT# assertion. Once the BINIT# assertion has been observed, the bus agents will re-arbitrate for the front side bus and attempt completion of their bus queue and IOQ entries. If BINIT# observation is enabled during power on configuration, a central agent may handle an assertion of BINIT# as appropriate to the error handling architecture of the system.
BNR#	I/O	BNR# (Block Next Request) is used to assert a bus stall by any bus agent who is unable to accept new bus transactions. During a bus stall, the current bus owner cannot issue any new transactions. Since multiple agents might need to request a bus stall at the same time, BNR# is a wire-OR signal which must connect the appropriate pins of all processor system bus agents. In order to avoid wire-OR glitches associated with simultaneous edge transitions driven by multiple drivers, BNR# is activated on specific clock edges and sampled on specific clock edges.
BOOT_ SELECT	I	The BOOT_SELECT input informs the processor whether the platform supports the processor. Incompatible platform designs will have this input connected to V_{SS}. Thus, this pin is essentially an electrical key to prevent the processor from running in a system that is not designed for it. For platforms that are designed to support the 64-bit Intel® Xeon™ processor MP with up to 8MB L3 cache, this pin should be a no-connect.
BPM[5:0]#	I/O	BPM[5:0]# (Breakpoint Monitor) are breakpoint and performance monitor signals. They are outputs from the processor which indicate the status of breakpoints and programmable counters used for monitoring processor performance. BPM[5:0]# should connect the appropriate pins of all processor front side bus agents. BPM4# provides PRDY# (Probe Ready) functionality for the TAP port. PRDY# is a processor output used by debug tools to determine processor debug readiness. BPM5# provides PREQ# (Probe Request) functionality for the TAP port. PREQ# is a processor input and is used by debug tools to request debug operation of the processors. BPM[5:4]# must be bussed to all bus agents.
BPRI#	I	BPRI# (Bus Priority Request) is used to arbitrate for ownership of the processor front side bus. It must connect the appropriate pins of all processor front side bus agents. Observing BPRI# active (as asserted by the priority agent) causes all other agents to stop issuing new requests, unless such requests are part of an ongoing locked operation. The priority agent keeps BPRI# asserted until its requests are issued, then releases the bus by deasserting BPRI#.

Table 6-1. Signal Definitions (Sheet 3 of 9)

Name	Type	Description
BR0# BR[3:1]#	I/O I	BR[3:0]# (Bus Request) drive the BREQ[3:0]# signals in the system. The BREQ[3:0]# signals are interconnected in a rotating manner to individual processor pins. The tables below give the rotating interconnect between the processor and bus signals for 3-load configurations. **BR[1:0]# Signals Rotating Interconnect, 3-Load Configuration** Bus Signal / Agent 0 Pins / Agent 1 Pins BREQ0# / BR0# / BR1# BREQ1# / BR1# / BR0# BR2# and BR3# must not be utilized in 3-load configurations. However, they must still be terminated. During power-on configuration, the central agent must assert the BR0# bus signal. All symmetric agents sample their BR[3:0]# pins on the active-to-inactive transition of RESET#. The pin which the agent samples asserted determines its agent ID.
BSEL[1:0]	O	These output signals are used to select the front side bus frequency. The frequency is determined by the processor(s), chipset, and frequency synthesizer capabilities. All front side bus agents must operate at the same frequency. Individual processors will only operate at their specified front side bus frequency. See Table 2-2 for output values.
COMP0	I	COMP0 must be terminated to V_{SS} on the baseboard using precision resistors. This input configures the AGTL+ drivers of the processor. Refer to Table 2-19.
CVID[3:0]	O	CVID[3:0] (Cache Voltage ID) pins are used to support automatic selection of V_{CACHE}. These are open drain signals that are driven by the processor and must be pulled to no more than 3.3 V (+5% tolerance) with a resistor. Conversely, the V_{CACHE} VR output must be disabled prior to the voltage supply for these pins becoming invalid. The CVID pins are needed to support processor voltage specification variations. See Table 2-4 for definitions of these pins. The V_{CACHE} VR must supply the voltage that is requested by these pins, or disable itself.
D[63:0]#	I/O	D[63:0]# (Data) are the data signals. These signals provide a 64-bit data path between the processor front side bus agents, and must connect the appropriate pins on all such agents. The data driver asserts DRDY# to indicate a valid data transfer. D[63:0]# are quad-pumped signals, and will thus be driven four times in a common clock period. D[63:0]# are latched off the falling edge of both DSTBP[3:0]# and DSTBN[3:0]#. Each group of 16 data signals correspond to a pair of one DSTBP# and one DSTBN#. The following table shows the grouping of data signals to strobes and DBI#. Furthermore, the DBI# pins determine the polarity of the data signals. Each group of 16 data signals corresponds to one DBI# signal. When the DBI# signal is active, the corresponding data group is inverted and therefore sampled active high.
DBI[3:0]#	I/O	DBI[3:0]# are source synchronous and indicate the polarity of the D[63:0]# and DEP[7:0]# signals. The DBI[3:0]# signals are activated when the data on the data bus is inverted. If more than half the data bits, within an 18-bit group (including ECC bits), would have been asserted electrically low, the bus agent may invert the data bus and corresponding ECC signals for that particular sub-phase for that 18-bit group.

Table 6-1. Signal Definitions (Sheet 4 of 9)

Name	Type	Description
DBSY#	I/O	DBSY# (Data Bus Busy) is asserted by the agent responsible for driving data on the processor front side bus to indicate that the data bus is in use. The data bus is released after DBSY# is deasserted. This signal must connect the appropriate pins on all processor front side bus agents.
DEFER#	I	DEFER# is asserted by an agent to indicate that a transaction cannot be guaranteed in-order completion. Assertion of DEFER# is normally the responsibility of the addressed memory or I/O agent. This signal must connect the appropriate pins of all processor front side bus agents.
DEP[7:0]#	I/O	The DEP[7:0]# (data bus ECC protection) signals provide optional ECC protection for the data bus. They are driven by the agent responsible for driving D[63:0]#, and, if ECC is implemented, must connect the appropriate pins of all bus agents which use them. Furthermore, the DBI# pins determine the polarity of the ECC signals. Each pair of 2 ECC signals corresponds to one DBI# signal. When the DBI# signal is active, the corresponding ECC pair is inverted and therefore sampled active high.
DP[3:0]#	I/O	DP[3:0]# (Data Parity) provide optional parity protection for the data bus. They are driven by the agent responsible for driving D[63:0]#, and, if parity is implemented, must connect the appropriate pins of all bus agents which use them.
DRDY#	I/O	DRDY# (Data Ready) is asserted by the data driver on each data transfer, indicating valid data on the data bus. In a multi-common clock data transfer, DRDY# may be deasserted to insert idle clocks. This signal must connect the appropriate pins of all processor front side bus agents.
DSTBN[3:0]#	I/O	Data strobe used to latch in D[63:0]#, DEP[7:0]# and DBI[3:0]#.
DSTBP[3:0]#	I/O	Data strobe used to latch in D[63:0]#, DEP[7:0]# and DBI[3:0]#.
FERR#/PBE#	O	FERR#/PBE# (floating-point error/pending break event) is a multiplexed signal and its meaning is qualified by STPCLK#. When STPCLK# is not asserted, FERR#/PBE# indicates a floating-point error and will be asserted when the processor detects an unmasked floating-point error. When STPCLK# is not asserted, FERR#/PBE# is similar to the ERROR# signal on the Intel 387 coprocessor, and is included for compatibility with systems using MS-DOS*-type floating-point error reporting. When STPCLK# is asserted, an assertion of FERR#/PBE# indicates that the processor has a pending break event waiting for service. The assertion of FERR#/PBE# indicates that the processor should be returned to the Normal state. For additional information on the pending break event functionality, including the identification of support of the feature and enable/disable information, refer to Volume 3 of the *IA-32 Intel® Architecture Software Developer's Manual* and the *AP-485 Intel® Processor Identification and the CPUID Instruction* application note.
FORCEPR#	I	This input can be used to force activation of the Thermal Control Circuit.
GTLREF[3:0]	I	GTLREF determines the signal reference level for AGTL+ input pins. GTLREF is used by the AGTL+ receivers to determine if a signal is an electrical 0 or an electrical 1. Please refer to Table 2-19 for further details.
HIT# HITM#	I/O I/O	HIT# (Snoop Hit) and HITM# (Hit Modified) convey transaction snoop operation results. Any front side bus agent may assert both HIT# and HITM# together to indicate that it requires a snoop stall, which can be continued by reasserting HIT# and HITM# together, every other common clock. Since multiple agents may deliver snoop results at the same time, HIT# and HITM# are wire-OR signals which must connect the appropriate pins of all processor front side bus agents. In order to avoid wire-OR glitches associated with simultaneous edge transitions driven by multiple drivers, HIT# and HITM# are activated on specific clock edges and sampled on specific clock edges.

Table 6-1. Signal Definitions (Sheet 5 of 9)

Name	Type	Description
ID[7:0]#	I	ID[7:0]# are the Transaction ID signals. They are driven during the Deferred Phase by the deferring agent.
IDS#	I	IDS# is the ID Strobe signal. It is asserted to begin the Deferred Phase.
IERR#	O	IERR# (Internal Error) is asserted by a processor as the result of an internal error. Assertion of IERR# is usually accompanied by a SHUTDOWN transaction on the processor front side bus. This transaction may optionally be converted to an external error signal (e.g., NMI) by system core logic. The processor will keep IERR# asserted until the assertion of RESET#.
IGNNE#	I	IGNNE# (Ignore Numeric Error) is asserted to force the processor to ignore a numeric error and continue to execute noncontrol floating-point instructions. If IGNNE# is deasserted, the processor generates an exception on a noncontrol floating-point instruction if a previous floating-point instruction caused an error. IGNNE# has no effect when the NE bit in control register 0 (CR0) is set. IGNNE# is an asynchronous signal. However, to ensure recognition of this signal following an I/O write instruction, it must be valid a 6 clks before the I/O write's response.
INIT#	I	INIT# (Initialization), when asserted, resets integer registers inside all processors without affecting their internal caches or floating-point registers. Each processor then begins execution at the power-on Reset vector configured during power-on configuration. The processor continues to handle snoop requests during INIT# assertion. INIT# is an asynchronous signal and must connect the appropriate pins of all processor front side bus agents. If INIT# is sampled active on the active to inactive transition of RESET#, then the processor executes its Built-in Self-Test (BIST).
LINT0/INTR LINT1/NMI	I	LINT[1:0] (Local APIC Interrupt) must connect the appropriate pins of all front side bus agents. When the APIC functionality is disabled, the LINT0 signal becomes INTR, a maskable interrupt request signal, and LINT1 becomes NMI, a nonmaskable interrupt. INTR and NMI are backward compatible with the signals of those names on the Pentium® processor. Both signals are asynchronous. These signals must be software configured via BIOS programming of the APIC register space to be used either as NMI/INTR or LINT[1:0]. Because the APIC is enabled by default after Reset, operation of these pins as LINT[1:0] is the default configuration.
LOCK#	I/O	LOCK# indicates to the system that a set of transactions must occur atomically. This signal must connect the appropriate pins of all processor front side bus agents. For a locked sequence of transactions, LOCK# is asserted from the beginning of the first transaction to the end of the last transaction. When the priority agent asserts BPRI# to arbitrate for ownership of the processor front side bus, it will wait until it observes LOCK# deasserted. This enables symmetric agents to retain ownership of the processor front side bus throughout the bus locked operation and ensure the atomicity of lock.

Table 6-1. Signal Definitions (Sheet 6 of 9)

Name	Type	Description
MCERR#	I/O	MCERR# (Machine Check Error) is asserted to indicate an unrecoverable error or a bus protocol violation. It may be driven by all processor front side bus agents. MCERR# assertion conditions are configurable at a system level. Assertion options are defined as follows: • Enabled or disabled. • Asserted, if configured, for internal errors along with IERR#. • Asserted, if configured, by the request initiator of a bus transaction after it observes an error. • Asserted by any bus agent when it observes an error in a bus transaction. For more details regarding machine check architecture, refer to the *IA-32 Intel® Software Developer's Manual, Volume 3: System Programming Guide*. Since multiple agents may drive this signal at the same time, MCERR# is a wired-OR signal which must connect the appropriate pins of all processor front side bus agents. In order to avoid wire-OR glitches associated with simultaneous edge transitions driven by multiple drivers, MCERR# is activated on specific clock edges and sampled on specific clock edges.
ODTEN	I	ODTEN (On-die termination enable) should be connected to V_{TT} through a resistor to enable on-die termination for end bus agents. For middle bus agents, pull this signal down via a resistor to ground to disable on-die termination. Whenever ODTEN is high, on-die termination will be active, regardless of other states of the bus.
OOD#	I	OOD# allows data delivery to occur subsequent to IDS# assertion during the Deferred Phase.
PROCHOT#	O	The assertion of PROCHOT# (processor hot) indicates that the processor die temperature has reached its thermal limit. See Section 7.2.4 for more details.
PWRGOOD	I	PWRGOOD (Power Good) is an input. The processor requires this signal to be a clean indication that all processor clocks and power supplies are stable and within their specifications. "Clean" implies that the signal will remain low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until they come within specification. The signal must then transition monotonically to a high state. Figure 2-18 illustrates the relationship of PWRGOOD to the RESET# signal. PWRGOOD can be driven inactive at any time, but clocks and power must again be stable before a subsequent rising edge of PWRGOOD. It must also meet the minimum pulse width specification in Table 2-21, and be followed by a 1 ms active RESET# pulse. The PWRGOOD signal must be supplied to the processor. This signal is used to protect internal circuits against voltage sequencing issues. It should be driven high throughout boundary scan operation.
REQ[4:0]#	I/O	REQ[4:0]# (Request Command) must connect the appropriate pins of all processor front side bus agents. They are asserted by the current bus owner to define the currently active transaction type. These signals are source synchronous to ADSTB[1:0]#. Refer to the AP[1:0]# signal description for details on parity checking of these signals.
RESET#	I	Asserting the RESET# signal resets all processors to known states and invalidates their internal caches without writing back any of their contents. For a power-on Reset, RESET# must stay active for at least 1 ms after V_{CC} and BCLK have reached their specified levels. On observing active RESET#, all front side bus agents will deassert their outputs within two clocks. RESET# must not be kept asserted for more than 10 ms. A number of bus signals are sampled at the active-to-inactive transition of RESET# for power-on configuration. These configuration options are described in Section 8.1.

Table 6-1. Signal Definitions (Sheet 7 of 9)

Name	Type	Description
RS[2:0]#	I	RS[2:0]# (Response Status) are driven by the response agent (the agent responsible for completion of the current transaction), and must connect to the appropriate pins of all processor front side bus agents.
RSP#	I	RSP# (Response Parity) is driven by the response agent (the agent responsible for completion of the current transaction) during assertion of RS[2:0]#, the signals for which RSP# provides parity protection. It must connect to the appropriate pins of all processor front side bus agents. A correct parity signal is electrically high if an even number of covered signals are electrically low and electrically low if an odd number of covered signals are electrically low. If RS[2:0]# are all electrically high, RSP# is also electrically high, since this indicates it is not being driven by any agent guaranteeing correct parity.
SKTOCC#	O	SKTOCC# (Socket occupied) will be pulled to ground by the processor to indicate that the processor is present. There is no connection to the processor silicon for this signal.
SLEW_CTRL	I	SLEW_CTRL must be terminated to V_{SS} on the baseboard using precision resistors. This input configures the slew rate of the AGTL+ drivers. Refer to Table 2-19 for implementation details.
SM_ALERT#	O	SM_ALERT# (SMBus Alert) is an asynchronous interrupt line associated with the SMBus Thermal Sensor device. It is an open-drain output and the processor includes a 10kΩ pull-up resistor to SM_VCC for this signal. For more information on the usage of the SM_ALERT# pin, see Section 8.4.7.
SM_CLK	I/O	The SM_CLK (SMBus Clock) signal is an input clock to the system management logic which is required for operation of the system management features of the processor. This clock is driven by the SMBus controller and is asynchronous to other clocks in the processor.The processor includes a 10 kΩ pull-up resistor to SM_VCC for this signal.
SM_DAT	I/O	The SM_DAT (SMBus Data) signal is the data signal for the SMBus. This signal provides the single-bit mechanism for transferring data between SMBus devices. The processor includes a 10k Ω pull-up resistor to SM_VCC for this signal.
SM_EP_A[2:0]	I	The SM_EP_A (EEPROM Select Address) pins are decoded on the SMBus in conjunction with the upper address bits in order to maintain unique addresses on the SMBus in a system with multiple processors. To set an SM_EP_A line high, a pull-up resistor should be used that is no larger than 1 kΩ. The processor includes a 10 kΩ pull-down resistor to V_{SS} for each of these signals. For more information on the usage of these pins, see Section 8.4.8.
SM_TS_A[1:0]	I	The SM_TS_A (Thermal Sensor Select Address) pins are decoded on the SMBus in conjunction with the upper address bits in order to maintain unique addresses on the SMBus in a system with multiple processors. The device's addressing, as implemented, includes a Hi-Z state for both address pins. The use of the Hi-Z state is achieved by leaving the input floating (unconnected). For more information on the usage of these pins, see Section 8.4.8.
SM_VCC	I	SM_VCC provides power to the SMBus components on the processor package.
SM_WP	I	WP (Write Protect) can be used to write protect the Scratch EEPROM. The Scratch EEPROM is write-protected when this input is pulled high to SM_VCC. The processor includes a 10 kΩ pull-down resistor to V_{SS} for this signal.

Table 6-1. Signal Definitions (Sheet 8 of 9)

Name	Type	Description
SMI#	I	SMI# (System Management Interrupt) is asserted asynchronously by system logic. On accepting a System Management Interrupt, processors save the current state and enter System Management Mode (SMM). An SMI Acknowledge transaction is issued, and the processor begins program execution from the SMM handler. It is required that SMI# assertion be observed 8 BCLKs before the Response Status (RS[2:0]#) is observed by the processor. If SMI# is asserted during the deassertion of RESET#, the processor will tri-state its outputs.
STPCLK#	I	STPCLK# (Stop Clock), when asserted, causes processors to enter a low power Stop-Grant state. The processor issues a Stop-Grant Acknowledge transaction, and stops providing internal clock signals to all processor core units except the front side bus and APIC units. The processor continues to snoop bus transactions and service interrupts while in Stop-Grant state. When STPCLK# is deasserted, the processor restarts its internal clock to all units and resumes execution. The assertion of STPCLK# has no effect on the bus clock; STPCLK# is an asynchronous input.
TCK	I	TCK (Test Clock) provides the clock input for the processor Test Access Port.
TDI	I	TDI (Test Data In) transfers serial test data into the processor. TDI provides the serial input needed for JTAG specification support.
TDO	O	TDO (Test Data Out) transfers serial test data out of the processor. TDO provides the serial output needed for JTAG specification support.
TEST_BUS	I	Must be connected to all other processor TEST_BUS signals in the system.
TESTHI[6:0]	I	TESTHI[6:0] must be connected to a V_{TT} power source through a resistor for proper processor operation. See Section 2.4 for more details.
THERMTRIP#	O	Assertion of THERMTRIP# (Thermal Trip) indicates the processor junction temperature has reached a temperature beyond which permanent silicon damage may occur. THERMTRIP# (Thermal Trip) will activate at a temperature that is approximately 20°C above the maximum case temperature (T_C). Measurement of the temperature is accomplished through an internal thermal sensor. Upon assertion of THERMTRIP#, the processor will shut off its internal clocks (thus halting program execution) in an attempt to reduce the processor junction temperature. To protect the processor its core voltage (V_{CC}) must be removed following the assertion of THERMTRIP#. See Figure 2-15 and Table 2-23 for the appropriate power down sequence and timing requirements. Driving of the THERMTRIP# signals is enabled within 10 µs of the assertion of PWRGOOD and is disabled on de-assertion of PWRGOOD. Once activated, THERMTRIP# remains latched until PWRGOOD is de-asserted. While the de-assertion of the PWRGOOD signal will de-assert THERMTRIP#, if the processor's junction temperature remains at or above the trip level, THERMTRIP# will again be asserted within 10 µs of the assertion of PWRGOOD. Thermtrip should not be sampled until 10 µs after PWRGOOD assertion at the processor.
TMS	I	TMS (Test Mode Select) is a JTAG specification support signal used by debug tools.
TRDY#	I	TRDY# (Target Ready) is asserted by the target (chipset) to indicate that it is ready to receive a write or implicit writeback data transfer. TRDY# must connect the appropriate pins of all front side bus agents.
TRST#	I	TRST# (Test Reset) resets the Test Access Port (TAP) logic. TRST# must be driven electrically low during power on Reset.
V_{CACHE}	I	V_{CACHE} provides power to the L3 cache on the processor.
V_{CC}	I	V_{CC} provides power to the core logic of the processor.

Table 6-1. Signal Definitions (Sheet 9 of 9)

Name	Type	Description
V_{CCA}	I	V_{CCA} provides isolated power for the analog portion of the internal PLL's. Use a discrete RLC filter to provide clean power.
V_{CCA_CACHE}	I	V_{CCA_CACHE} provides isolated power for the L3 cache PLL. Use a discrete RLC filter to provide clean power.
$V_{CC\_CACHE\_SENSE}$ $V_{SS\_CACHE\_SENSE}$	O	$V_{CC\_CACHE\_SENSE}$ and $V_{SS\_CACHE\_SENSE}$ provide isolated, low impedance connections to the processor cache voltage (V_{CACHE}) and ground (V_{SS}). They can be used to sense or measure voltage or ground near the silicon with little noise.
$V_{CCIOPLL}$	I	$V_{CCIOPLL}$ provides isolated power for digital portion of the internal PLL's.
V_{CCPLL}	I	The on-die PLL filter solution will not be implemented on this platform. The V_{CCPLL} input should be left unconnected.
$V_{CCSENSE}$ $V_{SSSENSE}$	O	$V_{CCSENSE}$ and $V_{SSSENSE}$ provide isolated, low impedance connections to the processor core voltage (V_{CC}) and ground (V_{SS}). These signals must be connected to the voltage regulator feedback signals, which ensure the output voltage (i.e. processor voltage) remains within specification.
VID[5:0]	O	VID[5:0] (Voltage ID) pins are used to support automatic selection of V_{CC}. These are open drain signals that are driven by the processor and must be pulled to no more than 3.3 V (+5% tolerance) with a resistor. Conversely, the V_{CC} VR output must be disabled prior to the voltage supply for these pins becoming invalid. The VID pins are needed to support processor voltage specification variations. See Table 2-3 for definitions of these pins. The V_{CC} VR must supply the voltage that is requested by these pins, or disable itself.
VIDPWRGD	I	The processor requires this input to determine that the supply voltage for BSEL[1:0], VID[5:0], and CVID[3:0] is stable and within specification.
V_{SS}	I	V_{SS} is the ground plane for the processor.
V_{SSA}	I	V_{SSA} provides an isolated, **internal** ground for internal PLL's. Do not connect directly to ground. This pin is to be connected to V_{CCA} and $V_{CCIOPLL}$ through a discrete filter circuit.
V_{SSA_CACHE}	I	V_{SSA_CACHE} provides an isolated, **internal** ground for the L3 cache PLL. Do not connect directly to ground.
V_{TT}	I	V_{TT} is the front side bus termination voltage.
VTTEN	O	VTTEN can be used as an output enable for the V_{TT} regulator. VTTEN is used as an electrical key to prevent processors with mechanically-equivalent pinouts from accidentally booting in a 64-bit Intel® Xeon™ processor MP with up to 8MB L3 cache platform. Since VTTEN is an open circuit on the processor package, VTTEN must be pulled up on the motherboard.

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7 Thermal Specifications

7.1 Package Thermal Specifications

The 64-bit Intel® Xeon™ processor MP with up to 8MB L3 cache requires a thermal solution to maintain temperatures within operating limits. Any attempt to operate the processor outside these operating limits may result in permanent damage to the processor and potentially other components within the system. As processor technology changes, thermal management becomes increasingly crucial when building computer systems. Maintaining the proper thermal environment is key to reliable, long-term system operation.

A complete solution includes both component and system level thermal management features. Component level thermal solutions can include active or passive heatsinks attached to the processor Integrated Heat Spreader (IHS). Typical system level thermal solutions may consist of system fans combined with ducting and venting.

For more information on designing a component level thermal solution, refer to the Processor Thermal/Mechanical Design Guidelines.

Note: The boxed processor will ship with a component thermal solution. Refer to Section 9 for details on the boxed processor.

7.1.1 Thermal Specifications

To allow the optimal operation and long-term reliability of Intel processor-based systems, the processor must remain within the minimum and maximum case temperature (T_{CASE}) specifications as defined by the applicable thermal profile (see Table 7-1 and Figure 7-1). Thermal solutions not designed to provide this level of thermal capability may affect the long-term reliability of the processor and system.

The 64-bit Intel® Xeon™ processor MP with up to 8MB L3 cache introduces a new methodology for managing processor temperatures which is intended to support acoustic noise reduction through fan speed control and assure processor reliability. Selection of the appropriate fan speed will be based on the temperature reported by the processor's Thermal Diode. If the diode temperature is greater than or equal to Tcontrol (see Section 7.2.7), then the processor case temperature must remain at or below the temperature as specified by the thermal profile (see Figure 7-1). If the diode temperature is less than Tcontrol, then the case temperature is permitted to exceed the thermal profile, but the diode temperature must remain at or below Tcontrol. Systems that implement fan speed control must be designed to take these conditions into account. Systems that do not alter the fan speed only need to guarantee the case temperature meets the thermal profile specifications.

The processor thermal profile ensures adherence to Intel reliability requirements. The thermal profile is representative of a volumetrically unconstrained thermal solution (i.e. industry enabled 2U+ heat sink). In this scenario, it is expected that the Thermal Control Circuit (TCC) would only be activated for very brief periods of time when running the most power intensive applications.

The upper point of the thermal profile consists of the Thermal Design Power (TDP) defined in Table 7-1 and the associated T_{CASE} value. The lower point of the thermal profile consists of x = $P_{CONTROL\_BASE}$ and y = T_{CASE_MAX} @ $P_{CONTROL\_BASE}$. Pcontrol is defined as the processor

power at which T_{CASE}, calculated from the thermal profile, corresponds to the lowest possible value of Tcontrol. This point is associated with the Tcontrol value (see Section 7.2.7). However, because Tcontrol represents a diode temperature, it is necessary to define the associated case temperature. This is T_{CASE_MAX} @ $P_{CONTROL\_BASE}$. Please see Section 7.2.7 and the Processor Thermal/Mechanical Design Guidelines for proper usage of the Tcontrol specification.

The case temperature is defined at the geometric top center of the processor IHS. Analysis indicates that real applications are unlikely to cause the processor to consume maximum power dissipation for sustained time periods. Intel recommends that complete thermal solution designs target the TDP indicated in Table 7-1, instead of the maximum processor power consumption. The Thermal Monitor feature is intended to help protect the processor in the event that an application exceeds the TDP recommendation for a sustained time period. For more details on this feature, refer to Section 7.2. To ensure maximum flexibility for future requirements, systems should be designed to the Flexible Motherboard (FMB) guidelines, even if a processor with a lower thermal dissipation is currently planned. **Thermal Monitor or Thermal Monitor 2 feature must be enabled for the processor to remain within specification.**

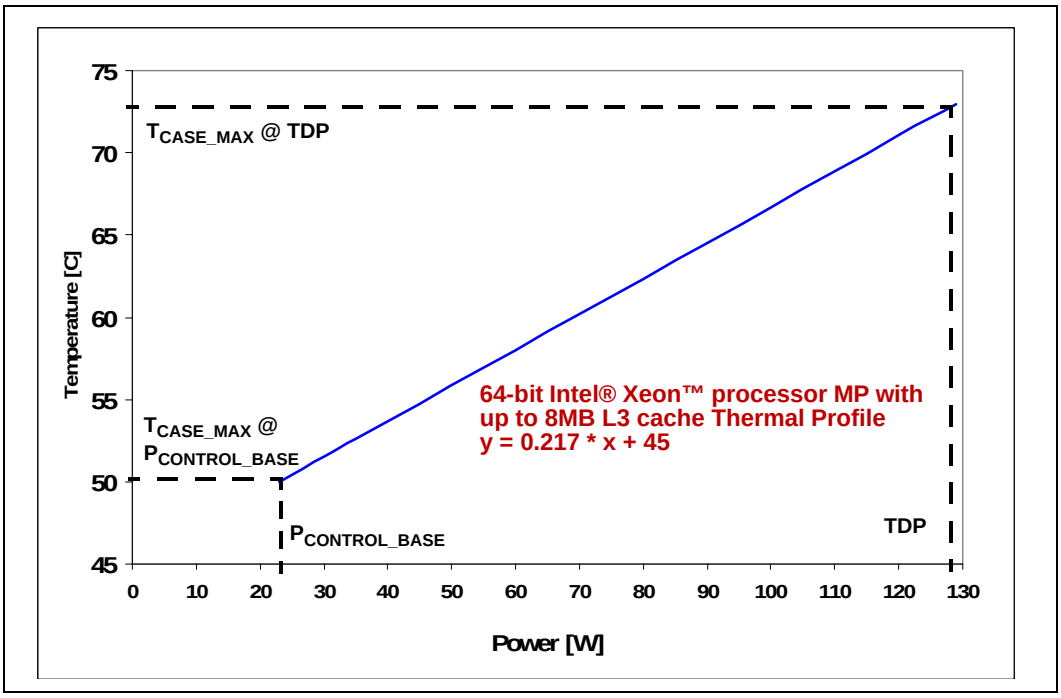
Table 7-1. Processor Thermal Specifications

Core Frequency	Maximum Power[3] (W)	Thermal Design Power (W)	Minimum T_{CASE} (°C)	Maximum T_{CASE} (°C)	Notes
Launch - FMB1	136	129	5	See Figure 7-1 and Table 7-2	1,2

NOTE:

1. Thermal Design Power (TDP) should be used for processor thermal solution design targets. The TDP is not the maximum power that the processor can dissipate. TDP is measured at maximum T_{CASE}.
2. FMB, or Flexible Motherboard, guidelines provide a design target for meeting future thermal requirements. See Section 2.10.1 for further information on FMB.
3. Maximum Power is the maximum thermal power that can be dissipated by the processor through the integrated heat spreader. Maximum Power is measured at maximum T_{CASE}.

Figure 7-1. 64-bit Intel® Xeon™ Processor MP with up to 8MB L3 Cache Thermal Profile



NOTE: Refer to the Processor Thermal/Mechanical Design Guidelines for system and environmental implementation details.

Table 7-2. 64-bit Intel® Xeon™ Processor MP with up to 8MB L3 Cache Thermal Profile

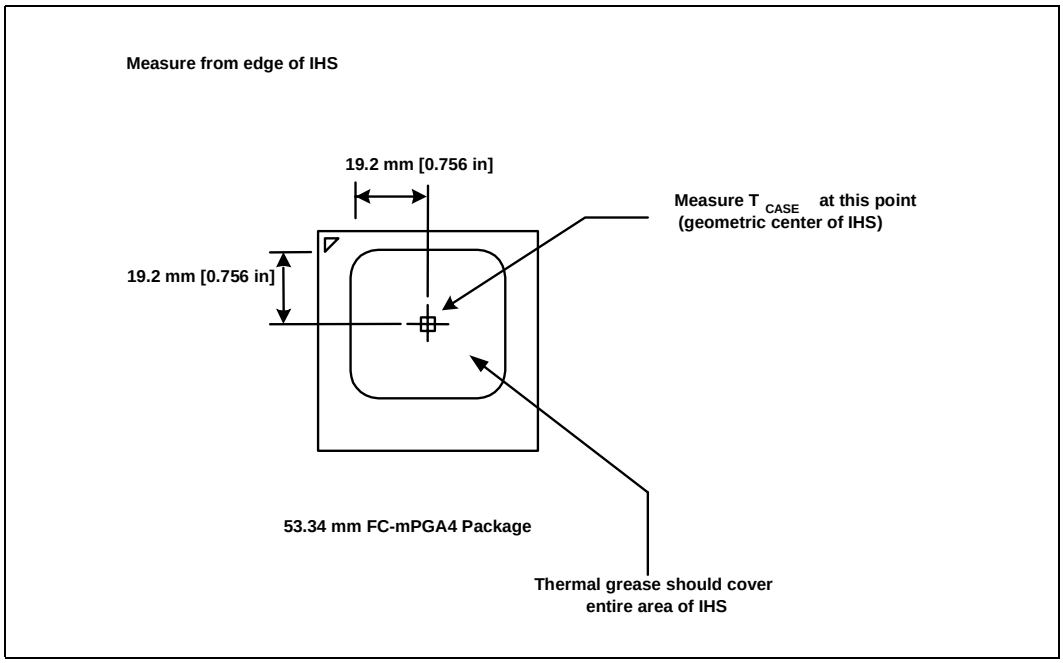
Power [W]	T_{CASE_MAX} [°C]
PCONTROL_BASE = 23	50
30	52
35	53
40	54
45	55
50	56
55	57
60	58
65	59
70	60
75	61

Power [W]	TCASE_MAX [°C]
80	62
85	63
90	65
95	66
100	67
105	68
110	69
115	70
120	71
125	72
129	73

7.1.2 Thermal Metrology

The maximum and minimum case temperatures (T_{CASE}) specified in Table 7-1 are measured at the geometric top center of the processor integrated heat spreader (IHS). Figure 7-2 illustrates the location where T_{CASE} temperature measurements should be made. For detailed guidelines on temperature measurement methodology, refer to the Processor Thermal/Mechanical Design Guidelines.

Figure 7-2. Case Temperature (T_{CASE}) Measurement Location



7.2 Processor Thermal Features

7.2.1 Thermal Monitor

The Thermal Monitor feature helps control the processor temperature by activating the Thermal Control Circuit (TCC) when the processor silicon reaches its maximum operating temperature. The TCC reduces processor power consumption as needed by modulating (starting and stopping) the internal processor core clocks. The Thermal Monitor (or Thermal Monitor 2) must be enabled for the processor to be operating within specifications. The temperature at which Thermal Monitor activates the thermal control circuit is not user configurable and is not software visible. Bus traffic is snooped in the normal manner, and interrupt requests are latched (and serviced during the time that the clocks are on) while the TCC is active.

When the Thermal Monitor is enabled and a high temperature situation exists (i.e. TCC is active), the clocks will be modulated by alternately turning the clocks off and on at a duty cycle specific to the processor (typically 30-50%). Clocks will not be off for more than 3 microseconds when the TCC is active. Cycle times are processor speed dependent and will decrease as processor core frequencies increase. A small amount of hysteresis has been included to prevent rapid active/

inactive transitions of the TCC when the processor temperature is near its maximum operating temperature. Once the temperature has dropped below the maximum operating temperature and the hysteresis timer has expired, the TCC goes inactive and clock modulation ceases.

With a thermal solution designed to meet the thermal profile, it is anticipated that the TCC would only be activated for very short periods of time when running the most power intensive applications. The processor performance impact due to these brief periods of TCC activation is expected to be so minor that it would be immeasurable. A thermal solution that is significantly under-designed may not be capable of cooling the processor even when the TCC is active continuously.

The duty cycle for the TCC, when activated by the Thermal Monitor, is factory configured and cannot be modified. The Thermal Monitor does not require any additional hardware, software drivers, or interrupt handling routines.

7.2.2 Thermal Monitor 2

The processor also supports an additional power reduction capability known as Thermal Monitor 2 (TM2). This mechanism provides an efficient means for limiting the processor temperature by reducing the power consumption within the processor. The Thermal Monitor (or Thermal Monitor 2) feature must be enabled for the processor to be operating within specifications.

When Thermal Monitor 2 is enabled and a high temperature situation is detected, the Thermal Control Circuit (TCC) will be activated. The TCC causes the processor to adjust its operating frequency (via the bus multiplier) and input voltage (via the VID signals). This combination of reduced frequency and VID results in a decrease to the processor power consumption.

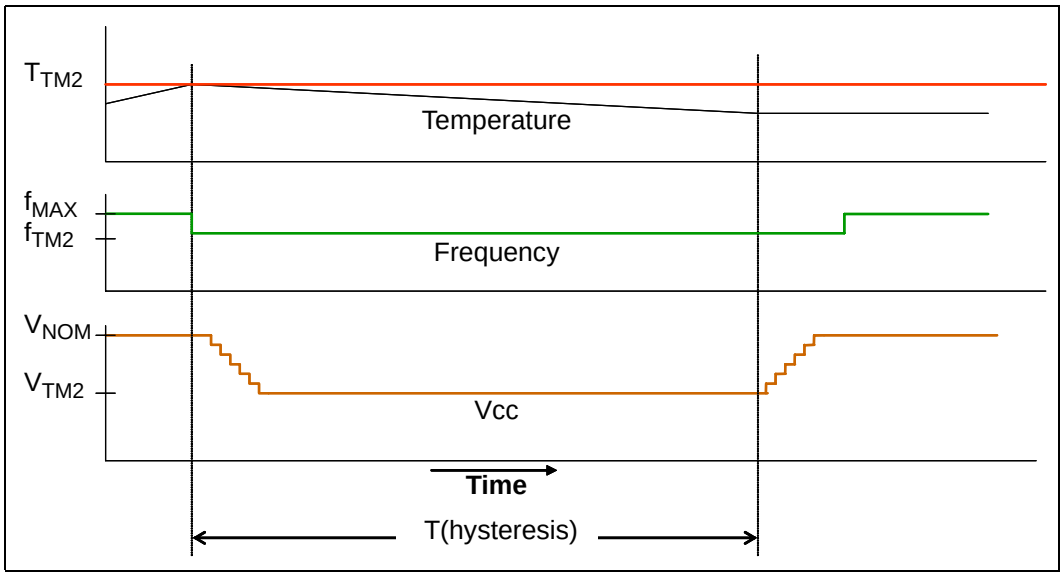
A processor enabled for Thermal Monitor 2 includes two operating points, each consisting of a specific operating frequency and voltage. The first operating point represents the normal operating condition for the processor. Under this condition, the core-frequency-to-system-bus multiplier utilized by the processor is that contained in the IA32_FLEX_BRVID_SEL MSR and the VID is that specified in Table 2-9. These parameters represent normal system operation.

The second point consists of both a lower operating frequency and voltage. When the TCC is activated, the processor automatically transitions to the new frequency. This transition occurs very rapidly (on the order of 5 microseconds). During the frequency transition, the processor is unable to service any bus requests, and consequently, all bus traffic is blocked. Edge-triggered interrupts will be latched and kept pending until the processor resumes operation at the new frequency.

Once the new operating frequency is engaged, the processor will transition to the new core operating voltage by issuing a new VID code to the voltage regulator. The voltage regulator must support dynamic VID steps in order to support Thermal Monitor 2. During the voltage change, it will be necessary to transition through multiple VID codes to reach the target operating voltage. Each step will be one VID table entry (see Table 2-9). The processor continues to execute instructions during the voltage transition. Operation at the lower voltage reduces the power consumption of the processor.

A small amount of hysteresis has been included to prevent rapid active/inactive transitions of the TCC when the processor temperature is near its maximum operating temperature. Once the temperature has dropped below the maximum operating temperature, and the hysteresis timer has expired, the operating frequency and voltage transition back to the normal system operating point. Transition of the VID code will occur first, in order to ensure proper operation once the processor reaches its normal operating frequency. Refer to Figure 7-3 for an illustration of this ordering.

Figure 7-3. Thermal Monitor 2 Frequency and Voltage Ordering



The PROCHOT# signal is asserted when a high temperature situation is detected, regardless of whether Thermal Monitor or Thermal Monitor 2 is enabled.

If a processor has its Thermal Control Circuit activated via a Thermal Monitor 2 event, and an Enhanced Intel SpeedStep‟ technology transition to a higher target frequency (through the applicable MSR write) is attempted, this frequency transition will be delayed until the TCC is deactivated and the TM2 event is complete.

7.2.3 On-Demand Mode

The processor provides an auxiliary mechanism that allows system software to force the processor to reduce its power consumption. This mechanism is referred to as “On-Demand” mode and is distinct from the Thermal Monitor and Thermal Monitor 2 features. On-Demand mode is intended as a means to reduce system level power consumption. Systems must not rely on software usage of this mechanism to limit the processor temperature.

If bit 4 of the IA_32_CLOCK_MODULATION MSR is written to a ‘1’, the processor will immediately reduce its power consumption via modulation (starting and stopping) of the internal core clock, independent of the processor temperature. When using On-Demand mode, the duty cycle of the clock modulation is programmable via bits 3:1 of the same IA_32_CLOCK_MODULATION MSR. In On-Demand mode, the duty cycle can be programmed from 12.5% on / 87.5% off to 87.5% on / 12.5% off in 12.5% increments. On-Demand mode may be used in conjunction with the Thermal Monitor or Thermal Monitor 2. If Thermal Monitor is enabled and the system tries to enable On-Demand mode at the same time the TCC is engaged, the factory configured duty cycle of the TCC will override the duty cycle selected by the On-Demand mode.

7.2.4 PROCHOT# Signal Pin

An external signal, PROCHOT# (processor hot), is asserted when the processor die temperature has reached its factory configured trip point. If the Thermal Monitor is enabled (note that the Thermal Monitor must be enabled for the processor to be operating within specification), the TCC will be active when PROCHOT# is asserted. The processor can be configured to generate an interrupt upon the assertion or de-assertion of PROCHOT#. Refer to the *Intel Architecture Software Developer's Manual* and the Processor BIOS Writers Guide for specific register and programming details.

PROCHOT# is designed to assert at or a few degrees higher than maximum T_{CASE} (as specified by the thermal profile) when dissipating TDP power, and cannot be interpreted as an indication of processor case temperature. This temperature delta accounts for processor package, lifetime, and manufacturing variations and attempts to ensure the Thermal Control Circuit is not activated below maximum T_{CASE} when dissipating TDP power. There is no defined or fixed correlation between the PROCHOT# trip temperature, the case temperature, or the thermal diode temperature. Thermal solutions must be designed to the processor specifications and cannot be adjusted based on experimental measurements of T_{CASE}, PROCHOT#, or Tdiode on random processor samples.

7.2.5 FORCEPR# Signal Pin

The FORCEPR# (force power reduction) input can be used by the platform to force the processor to activate the TCC. If the Thermal Monitor is enabled, the TCC will be activated upon the assertion of the FORCEPR# signal. The TCC will remain active until the system deasserts FORCEPR#. FORCEPR# is an asynchronous input. FORCEPR# can be used to thermally protect other system components. To use the voltage regulator (VR) as an example, when the FORCEPR# pin is asserted, the TCC in the processor will activate, reducing the current consumption of the processor and the corresponding temperature of the VR.

It should be noted that assertion of FORCEPR# does not automatically assert PROCHOT#. As mentioned previously, the PROCHOT# signal is asserted when a high temperature situation is detected. A minimum pulse width of 500 microseconds is recommended when FORCEPR# is asserted by the system. Sustained activation of the FORCEPR# pin may cause noticeable platform performance degradation.

7.2.6 THERMTRIP# Signal Pin

Regardless of whether or not Thermal Monitor or Thermal Monitor 2 is enabled, in the event of a catastrophic cooling failure, the processor will automatically shut down when the silicon has reached an elevated temperature (refer to the THERMTRIP# definition in Table 6-1). At this point, the system bus signal THERMTRIP# will go active and stay active as described in Table 6-1. THERMTRIP# activation is independent of processor activity and does not generate any bus cycles. If THERMTRIP# is asserted, processor core voltage (V_{CC}) and cache voltage (V_{CACHE}) must be removed within the timeframe defined in Table 2-23 and Figure 2-15. Intel also recommends removal of V_{TT}.

7.2.7 $T_{CONTROL}$ and Fan Speed Reduction

$T_{CONTROL}$ is a temperature specification based on a temperature reading from the thermal sensor. The value for $T_{CONTROL}$ will be calibrated in manufacturing and configured for each processor. The $T_{CONTROL}$ temperature for a given processor can be obtained by reading the

IA32_TEMPERATURE_TARGET MSR in the processor. The $T_{CONTROL}$ value that is read from the IA32_TEMPERATURE_TARGET MSR must be converted from Hexadecimal to Decimal and added to a base value of 50 ×C.

The value of $T_{CONTROL}$ may vary from 0x00h to 0x1Eh.

When T_{DIODE} is above $T_{CONTROL}$, then T_{CASE} must be at or below T_{CASE_MAX} as defined by the thermal profile (see Figure 7-1 and Table 7-2). Otherwise, the processor temperature can be maintained at $T_{CONTROL}$.

7.2.8 Thermal Diode

The processor incorporates an on-die thermal diode. A thermal sensor located on the processor package monitors the die temperature of the processor for thermal management/long term die temperature change purposes. The thermal diode is separate from the Thermal Monitor's thermal sensor and cannot be used to predict the behavior of the Thermal Monitor.

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8 Features

8.1 Power-On Configuration Options

Several configuration options can be set by hardware. The processor samples its hardware configuration at reset, on the active-to-inactive transition of RESET#. For specifications on these options, refer to Table 8-1.

The sampled information configures the processor for subsequent operation. These configuration options can only be changed by another reset. All resets configure the processor. For reset purposes, the processor does not distinguish between a “warm” reset and a “power-on” reset.

Table 8-1. Power-On Configuration Option Pins

Configuration Option	Pin[1,2]
Output tri state	SMI# or A[39]# for Arb ID 3 (middle agent) A[36]# for Arb ID 0 (end agent)
Execute BIST (Built-In Self Test)	INIT# or A[3]#
In Order Queue de-pipelining (set IOQ depth to 1)	A[7]#
Disable MCERR# observation	A[9]#
Disable BINIT# observation	A[10]#
APIC cluster ID	A[12:11]#
Disable bus parking	A[15]#
Core Frequency-to-Front Side Bus Multiplier	A[21:16]#
Symmetric agent arbitration ID	BR[1:0]#
Disable Hyper-Threading Technology (HT Technology)	A[31]#

NOTE:
1. Asserting this signal during RESET# selects the corresponding option.
2. Address pins not identified in this table as configuration options should not be asserted during RESET#.

8.2 Clock Control and Low Power States

The processor allows the use of HALT and Stop-Grant states to reduce power consumption by stopping the clock to internal sections of the processor, depending on each particular state. See Figure 8-1 for a visual representation of the processor low power states.

The processor adds support for Enhanced HALT power down state. Refer to Figure 8-1 and the following sections.

The Stop-Grant state requires chipset and BIOS support on multiprocessor systems. In a multiprocessor system, all the STPCLK# signals are bussed together, thus all processors are affected in unison. The Hyper-Threading Technology feature adds the conditions that all logical processors share the same STPCLK# signal internally. When the STPCLK# signal is asserted, the

processor enters the Stop-Grant state, issuing a Stop-Grant Special Bus Cycle (SBC) for each processor or logical processor. The chipset needs to account for a variable number of processors asserting the Stop-Grant SBC on the bus before allowing the processor to be transitioned into one of the lower processor power states. Refer to the applicable chipset specification for more information.

8.2.1 Normal State

This is the normal operating state for the processor.

8.2.2 HALT or Enhanced Power Down State

The Enhanced HALT power down state is configured and enabled via the BIOS. If the Enhanced HALT state is not enabled, the default power down state entered will be HALT. Refer to the section below for details on HALT and Enhanced HALT states.

8.2.2.1 HALT Power Down State

HALT is a low power state entered when all logical processors have executed the HALT or MWAIT instruction. When one of the logical processors executes the HALT or MWAIT instruction, that logical processor is halted; however, the other processor continues normal operation. The processor transitions to the Normal state upon the occurrence of SMI#, BINIT#, INIT#, LINT[1:0] (NMI, INTR), or an interrupt delivered over the front side bus. RESET# causes the processor to immediately initialize itself.

The return from a System Management Interrupt (SMI) handler can be to either Normal Mode or the HALT Power Down state. See the *IA-32 Intel® Architecture Software Developer's Manual, Volume 3: System Programming Guide* for more information.

The system can generate a STPCLK# while the processor is in the HALT Power Down state. When the system deasserts the STPCLK# interrupt, the processor returns execution to the HALT state.

While in HALT Power Down state, the processor processes bus snoops and interrupts.

8.2.2.2 Enhanced HALT Power Down State

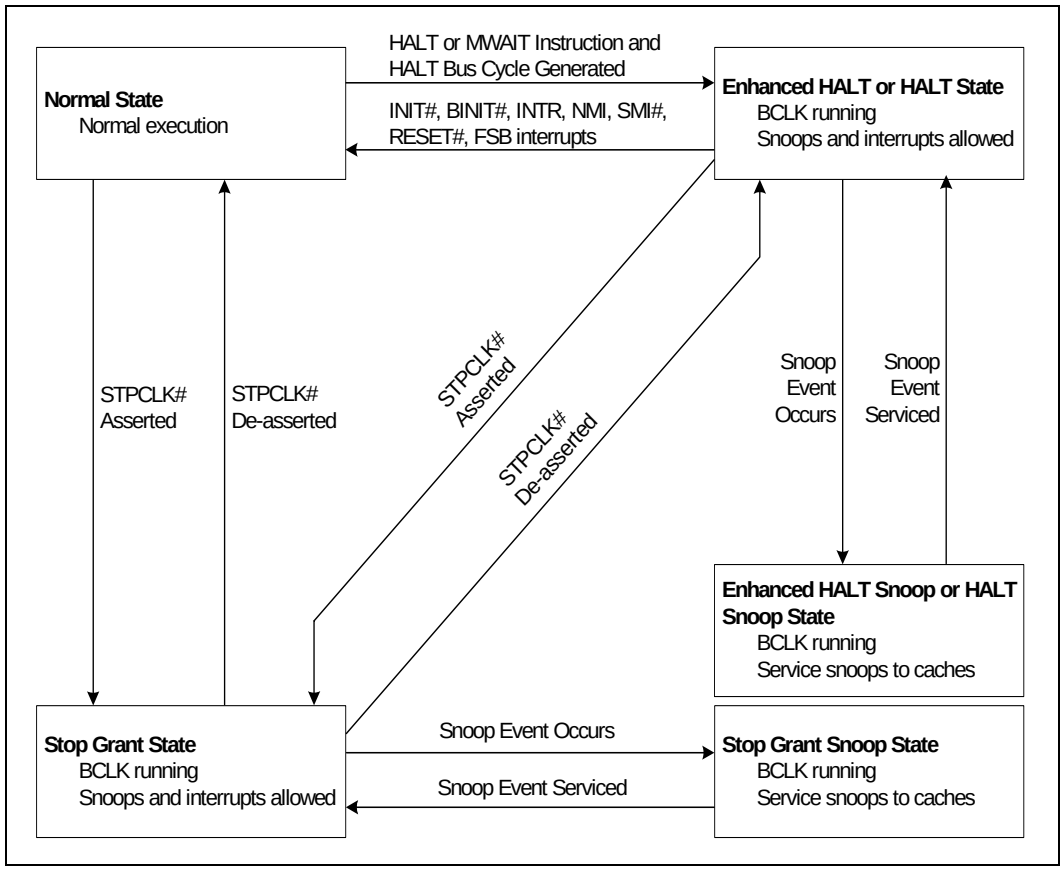
Enhanced HALT state is a low power state entered when all logical processors have executed the HALT or MWAIT instructions and Enhanced HALT state has been enabled via the BIOS. When one of the logical processors executes the HALT instruction, that logical processor is halted; however, the other processor continues normal operation. The Enhanced HALT state is generally a lower power state than the Stop Grant state.

The processor automatically transitions to a lower core frequency and voltage operating point before entering the Enhanced HALT state. Note that the processor FSB frequency is not altered; only the internal core frequency is changed. When entering the low power state, the processor first switches to the lower bus ratio and then transitions to the lower VID.

While in the Enhanced HALT state, the processor processes bus snoops.

The processor exits the Enhanced HALT state when a break event occurs. When the processor exits the Enhanced HALT state, it first transitions the VID to the original value and then changes the bus ratio back to the original value.

Figure 8-1. Stop Clock State Machine



8.2.3 Stop-Grant State

When the STPCLK# pin is asserted, the Stop-Grant state of the processor is entered 20 bus clocks after the response phase of the processor-issued Stop Grant Acknowledge special bus cycle. Both logical processors must be in the Stop-Grant state before the deassertion of STPCLK#.

Since the AGTL+ signal pins receive power from the front side bus, these pins should not be driven (allowing the level to return to V_{TT}) for minimum power drawn by the termination resistors in this state. In addition, all other input pins on the front side bus should be driven to the inactive state.

BINIT# is not serviced while the processor is in Stop-Grant state. The event is latched and can be serviced by software upon exit from the Stop-Grant state.

RESET# causes the processor to immediately initialize itself, but the processor will stay in Stop-Grant state. A transition back to the Normal state occurs with the deassertion of the STPCLK# signal.

A transition to the Grant Snoop state occurs when the processor detects a snoop on the front side bus (see Section 8.2.4).

While in the Stop-Grant state, SMI#, INIT#, BINIT# and LINT[1:0] are latched by the processor, and only serviced when the processor returns to the Normal state. Only one occurrence of each event is recognized upon return to the Normal state.

While in Stop-Grant state, the processor processes snoops on the front side bus and latches interrupts delivered on the front side bus.

The PBE# signal can be driven when the processor is in Stop-Grant state. PBE# is asserted if there is any pending interrupt latched within the processor. Pending interrupts that are blocked by the EFLAGS.IF bit being clear still cause assertion of PBE#. Assertion of PBE# indicates to system logic that it should return the processor to the Normal state.

8.2.4 Enhanced HALT Snoop State or HALT Snoop State, Stop Grant Snoop State

The Enhanced HALT Snoop state is used in conjunction with the Enhanced HALT state. If Enhanced HALT state is not enabled in the BIOS, the default Snoop state entered will be the HALT Snoop state. Refer to the sections below for details on HALT Snoop state, Grant Snoop state and Enhanced HALT Snoop state.

8.2.4.1 HALT Snoop State, Stop Grant Snoop State

The processor responds to snoop or interrupt transactions on the front side bus while in Stop-Grant state or in HALT Power Down state. During a snoop or interrupt transaction, the processor enters the HALT/Grant Snoop state. The processor stays in this state until the snoop on the front side bus has been serviced (whether by the processor or another agent on the front side bus) or the interrupt has been latched. After the snoop is serviced or the interrupt is latched, the processor will return to the Stop-Grant state or HALT Power Down state, as appropriate.

8.2.4.2 Enhanced HALT Snoop State

The Enhanced HALT Snoop state is the default Snoop state when the Enhanced HALT state is enabled via the BIOS. The processor remains in the lower bus ratio and VID operating point of the Enhanced HALT state.

While in the Enhanced HALT Snoop state, snoops and interrupt transactions are handled the same way as in the HALT Snoop state. After the snoop is serviced or the interrupt is latched, the processor returns to the Enhanced HALT state.

8.3 Enhanced Intel SpeedStep® Technology

Enhanced Intel SpeedStep technology enables the processor to switch between multiple frequency and voltage points, which may result in platform power savings. In order to support this technology, the system must support dynamic VID transitions. Switching between voltage/ frequency states is software controlled.

Note: Not all processors are capable of supporting Enhanced Intel SpeedStep technology. More details on which processor frequencies will support this feature will be provided in future releases of the Specification Update.

Enhanced Intel SpeedStep technology is a technology that creates processor performance states (P-states). P-states are power consumption and capability states within the Normal state. Enhanced Intel SpeedStep technology enables real-time dynamic switching between frequency and voltage points. It alters the performance of the processor by changing the bus to core frequency ratio and voltage. This allows the processor to run at different core frequencies and voltages to best serve the performance and power requirements of the processor and system. Note that the front side bus is not altered; only the internal core frequency is changed. In order to run at reduced power consumption, the voltage is altered in step with the bus ratio.

The following are key features of Enhanced Intel SpeedStep technology:

- Multiple voltage/frequency operating points provide optimal performance at reduced power consumption.
- Voltage/frequency selection is software controlled by writing to processor MSR's (Model Specific Registers), thus eliminating chipset dependency.
  - If the target frequency is higher than the current frequency, V_{CC} is incremented in steps (+12.5 mV) by placing a new value on the VID signals and the processor shifts to the new frequency. Note that the top frequency for the processor can not be exceeded.
  - If the target frequency is lower than the current frequency, the processor shifts to the new frequency and V_{CC} is then decremented in steps (-12.5 mV) by changing the target VID through the VID signals.

8.4 System Management Bus (SMBus) Interface

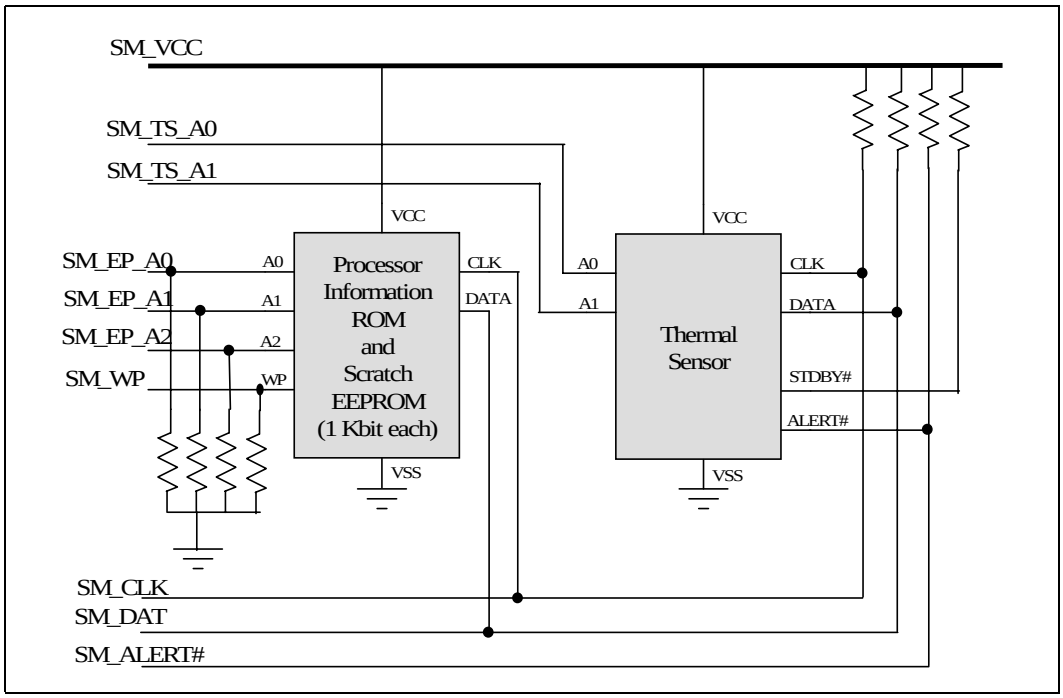
The processor package includes an SMBus interface which allows access to a memory component with two sections (referred to as the Processor Information ROM and the Scratch EEPROM) and a thermal sensor on the substrate. The SMBus thermal sensor may be used to read the thermal diode mentioned in Section 7.2.8. These devices and their features are described below.

The SMBus thermal sensor and its associated thermal diode are not related to and are completely independent of the precision, on-die temperature sensor and thermal control circuit (TCC) of the Thermal Monitor or Thermal Monitor 2 features discussed in Section 7.2.1.

The processor SMBus implementation uses the clock and data signals of the *System Management Bus (SMBus) Specification*. It does not implement the SMBSUS# signal.

For platforms which do not implement any of the SMBus features found on the processor, all of the SMBus connections, **except SM_VCC**, to the socket pins may be left unconnected (SM_ALERT#, SM_CLK, SM_DAT, SM_EP_A[2:0], SM_TS_A[1:0], SM_WP).

Figure 8-2. Logical Schematic of SMBus Circuitry



NOTE: Actual implementation may vary. This figure is provided to offer a general understanding of the architecture. All SMBus pull-up and pull-down resistors are 10 kΩ and located on the processor.

8.4.1 Processor Information ROM (PIROM)

The lower half (128 bytes) of the SMBus memory component is an electrically programmed read-only memory with information about the processor. This information is permanently write-protected. Table 8-2 shows the data fields and formats provided in the Processor Information ROM (PIROM).

Table 8-2. Processor Information ROM Format (Sheet 1 of 3)

Offset/Section	# of Bits	Function	Notes
Header:			
00h	8	Data Format Revision	Two 4-bit hex digits
01 - 02h	16	EEPROM Size	Size in bytes (MSB first)
03h	8	Processor Data Address	Byte pointer, 00h if not present
04h	8	Processor Core Data Address	Byte pointer, 00h if not present
05h	8	L3 Cache Data Address	Byte pointer, 00h if not present
06h	8	Package Data Address	Byte pointer, 00h if not present
07h	8	Part Number Data Address	Byte pointer, 00h if not present
08h	8	Thermal Reference Data Address	Byte pointer, 00h if not present

Table 8-2. Processor Information ROM Format (Sheet 2 of 3)

Offset/Section	# of Bits	Function	Notes
09h	8	Feature Data Address	Byte pointer, 00h if not present
0Ah	8	Other Data Address	Byte pointer, 00h if not present
0Bh	16	Reserved	Reserved
0Dh	8	Checksum	1 byte checksum
Processor Data:			
0E - 13h	48	S-spec/QDF Number	Six 8-bit ASCII characters
14h	6 2	Reserved Sample/Production	Reserved (most significant bits) 00b = Sample only, 01-11b = Production
15h	8	Checksum	1 byte checksum
Processor Core Data:			
16 - 17h	2	Processor Core Type	From CPUID
	4	Processor Core Family	From CPUID
	4	Processor Core Model	From CPUID
	4	Processor Core Stepping	From CPUID
	2	Reserved	Reserved for future use
18 - 19h	16	Reserved	Reserved for future use
1A - 1Bh	16	Front Side Bus Speed	16-bit binary number (in MHz)
1Ch	2 6	Multiprocessor Support Reserved	00b = UP,01b = DP,10b = RSVD,11b = MP Reserved
1D - 1Eh	16	Maximum Core Frequency	16-bit binary number (in MHz)
1F - 20h	16	Processor Core VID	V_{CC} requested by VID outputs in mV
21 - 22h	16	Core Voltage, Minimum	Minimum processor DC V_{CC} spec in mV
23h	8	T_{CASE} Maximum	Maximum case temperature spec in °C
24h	8	Checksum	1 byte checksum
Cache Data:			
25 - 26h	16	Reserved	Reserved for future use
27 - 28h	16	L2 Cache Size	16-bit binary number (in KB)
29 - 2Ah	16	L3 Cache Size	16-bit binary number (in KB)
2B - 2Ch	16	Processor Cache VID	V_{CACHE} requested by CVID outputs in mV
2D - 2Eh	16	Cache Voltage, Minimum	Minimum processor DC V_{CACHE} spec in mV
2F - 30h	16	Reserved	Reserved
31h	8	Checksum	1 byte checksum
Package Data:			
32 - 35h	32	Package Revision	Four 8-bit ASCII characters
36h	8	Reserved	Reserved for future use
37h	8	Checksum	1 byte checksum

Table 8-2. Processor Information ROM Format (Sheet 3 of 3)

Offset/Section	# of Bits	Function	Notes
Part Number Data:			
38 - 3Eh	56	Processor Part Number	Seven 8-bit ASCII characters
3F - 4Ch	112	Reserved	Reserved
4D - 54h	64	Processor Electronic Signature	64-bit identification number
55 - 6Eh	208	Reserved	Reserved
6Fh	8	Checksum	1 byte checksum
Thermal Ref. Data:			
70h	8	Reserved	Reserved
71 - 72h	16	Reserved	Reserved
73h	8	Reserved	Reserved
Feature Data:			
74 - 77h	32	Processor Core Feature Flags	From CPUID function 1, EDX contents
78h	8	Processor Feature Flags	[7] = Reserved [6] = Serial Signature [5] = Electronic Signature Present [4] = Thermal Sense Device Present [3] = Reserved [2] = OEM EEPROM Present [1] = Core VID Present [0] = L3 Cache Present
79-7Bh	24	Additional Processor Feature Flags	All bits Reserved
7Ch	8	Reserved	Reserved
7Dh	8	Checksum	1 byte checksum
Other Data:			
7E - 7Fh	16	Reserved	Reserved

8.4.2 Scratch EEPROM

Also available in the memory component on the processor SMBus is an EEPROM which may be used for other data at the system or processor vendor's discretion. The data in this EEPROM, once programmed, can be write-protected by asserting the active-high SM_WP signal. This signal has a weak pull-down (10 kW) to allow the EEPROM to be programmed in systems with no implementation of this signal. The Scratch EEPROM resides in the upper half of the memory component (addresses 80 - FFh). The lower half comprises the Processor Information ROM (addresses 00 - 7Fh), which is permanently write-protected by Intel.

8.4.3 PIROM and Scratch EEPROM Supported SMBus Transactions

The Processor Information ROM (PIROM) responds to two SMBus packet types: Read Byte and Write Byte. However, since the PIROM is write-protected, it will acknowledge a Write Byte command but ignore the data. The Scratch EEPROM responds to Read Byte and Write Byte commands. Table 8-3 diagrams the Read Byte command. Table 8-4 diagrams the Write Byte command. Following a write cycle to the scratch ROM, software must allow a minimum of 10 ms before accessing either ROM of the processor.

In the tables, 'S' represents the SMBus start bit, 'P' represents a stop bit, 'R' represents a read bit, 'W' represents a write bit, 'A' represents an acknowledge (ACK), and '///' represents a negative acknowledge (NACK). The shaded bits are transmitted by the Processor Information ROM or Scratch EEPROM, and the bits that aren't shaded are transmitted by the SMBus host controller. In the tables, the data addresses indicate 8 bits. The SMBus host controller should transmit 8 bits with the most significant bit indicating which section of the EEPROM is to be addressed: the Processor Information ROM (MSB = 0) or the Scratch EEPROM (MSB = 1).

Table 8-3. Read Byte SMBus Packet

S	Slave Address	Write	A	Command Code	A	S	Slave Address	Read	A	Data	///	P
1	7-bits	1	1	8-bits	1	1	7-bits	1	1	8-bits	1	1

Table 8-4. Write Byte SMBus Packet

S	Slave Address	Write	A	Command Code	A	Data	A	P
1	7-bits	1	1	8-bits	1	8-bits	1	1

8.4.4 SMBus Thermal Sensor

The processor's SMBus thermal sensor provides a means of acquiring thermal data from the processor. The thermal sensor is composed of control logic, SMBus interface logic, a precision analog-to-digital converter, and a precision current source. The sensor drives a small current through the p-n junction of a thermal diode located on the processor core. The forward bias voltage generated across the thermal diode is sensed and the precision A/D converter derives a single byte of thermal reference data, or a "thermal byte reading." The nominal precision of the least significant bit of a thermal byte is 1° Celsius.

The processor incorporates the SMBus thermal sensor onto the processor package. Upper and lower thermal reference thresholds can be individually programmed for the SMBus thermal sensor. Comparator circuits sample the register where the single byte of thermal data (thermal byte reading) is stored. These circuits compare the single-byte result against programmable threshold bytes. If enabled, the alert signal on the processor SMBus (SM_ALERT#) will be asserted when the sensor detects that either threshold is reached or crossed. Analysis of SMBus thermal sensor data may be useful in detecting changes in the system environment that may require attention.

The processor SMBus thermal sensor may be used to monitor long term temperature trends, but can not be used to manage the short term temperature of the processor or predict the activation of the thermal control circuit. As mentioned earlier, the processor's high thermal ramp rates make this infeasible. Refer to the thermal design guidelines listed in Section 1.2 for more details.

The SMBus thermal sensor feature in the processor cannot be used to measure T_{CASE}. The T_{CASE} specification in Section 7 must be met regardless of the reading of the processor's thermal sensor in order to ensure adequate cooling for the entire processor. The SMBus thermal sensor feature is only available while V_{CC} and SM_VCC are at valid levels and the processor is not in a low-power state.

8.4.5 Thermal Sensor Supported SMBus Transactions

The thermal sensor responds to five of the SMBus packet types: Write Byte, Read Byte, Send Byte, Receive Byte, and Alert Response Address (ARA). The Send Byte packet can be used for sending one-shot commands. The Receive Byte packet accesses the register commanded by the last Read Byte packet and can be used to continuously read from a register. If a Receive Byte packet was preceded by a Write Byte or send Byte packet more recently than a Read Byte packet, then the behavior is undefined. Table 8-5 through Table 8-9 diagram the five packet types. In these figures, 'S' represents the SMBus start bit, 'P' represents a stop bit, 'Ack' represents an acknowledge, and '///' represents a negative acknowledge (NACK). The shaded bits are transmitted by the thermal sensor, and the bits that aren't shaded are transmitted by the SMBus host controller. Table 8-10 shows the encoding of the command byte.

Table 8-5. Write Byte SMBus Packet

S	Slave Address	Write	Ack	Command Code	Ack	Data	Ack	P
1	7-bits	0	1	8-bits	1	8-bits	1	1

Table 8-6. Read Byte SMBus Packet

S	Slave Address	Write	Ack	Command Code	Ack	S	Slave Address	Read	Ack	Data	///	P
1	7-bits	0	1	8-bits	1	1	7-bits	1	1	8-bits	1	1

Table 8-7. Send Byte SMBus Packet

S	Slave Address	Write	Ack	Command Code	Ack	P
1	7-bits	0	1	8-bits	1	1

Table 8-8. Receive Byte SMBus Packet

S	Slave Address	Read	Ack	Data	///	P
1	7-bits	1	1	8-bits	1	1

Table 8-9. ARA SMBus Packet

S	ARA	Read	Ack	Address	///	P
1	0001 100	1	1	Device Address[1]	1	1

NOTE:
1. This is an 8-bit field. The device which sent the alert will respond to the ARA Packet with its address in the seven most significant bits. The least significant bit is undefined and may return as a '1' or '0'. See Section 8.4.8 for details on the Thermal Sensor Device addressing.

2. The shaded bits are transmitted by the thermal sensor, and the bits that aren't shaded are transmitted by the SMBus host controller.

Table 8-10. SMBus Thermal Sensor Command Byte Bit Assignments

Register	Command	Reset State	Function
RESERVED	00h	RESERVED	Reserved for future use
TRR	01h	0000 0000	Read processor core thermal diode
RS	02h	N/A	Read status byte (flags, busy signal)
RC	03h	00XX XXXX	Read configuration byte
RCR	04h	0000 0010	Read conversion rate byte
RESERVED	05h	RESERVED	Reserved for future use
RESERVED	06h	RESERVED	Reserved for future use
RRHL	07h	0111 1111	Read processor core thermal diode T_{HIGH} limit
RRLL	08h	1100 1001	Read processor core thermal diode T_{LOW} limit
WC	09h	N/A	Write configuration byte
WCR	0Ah	N/A	Write conversion rate byte
RESERVED	0Bh	RESERVED	Reserved for future use
RESERVED	0Ch	RESERVED	Reserved for future use
WRHL	0Dh	N/A	Write processor core thermal diode T_{HIGH} limit
WRLL	0Eh	N/A	Write processor core thermal diode T_{LOW} limit
OSHT	0Fh	N/A	One shot command (use send byte packet)
RESERVED	10h – FFh	N/A	Reserved for future use

All of the commands in Table 8-10 are for reading or writing registers in the SMBus thermal sensor, except the one-shot command (OSHT) register. The one-shot command forces the immediate start of a new conversion cycle. If a conversion is in progress when the one-shot command is received, then the command is ignored. If the thermal sensor is in stand-by mode when the one-shot command is received, a conversion is performed and the sensor returns to stand-by mode. The one-shot command is not supported when the thermal sensor is in auto-convert mode.

Note: Writing to a read-command register or reading from a write-command register will produce invalid results.

The default command after reset is to a reserved value (00h). After reset, Receive Byte SMBus packets will return invalid data until another command is sent to the thermal sensor.

8.4.6 SMBus Thermal Sensor Registers

8.4.6.1 Thermal Value Registers

Once the SMBus thermal sensor reads the processor thermal diode, it performs an analog to digital conversion and stores the results in the Thermal Reference Register (TRR). The supported range is +127 to 0 decimal and is expressed as an eight-bit number representing temperature in degrees

Celsius. This eight-bit value consists of seven bits of data and a sign bit (MSB) where the sign is always positive (sign = 0) and is shown in Table 8-11. The values shown are also used to program the Thermal Limit Registers.

The values of these registers should be treated as saturating values. Values above 127 are represented at 127 decimal, and values of zero and below may be represented as 0 to -127 decimal. If the device returns a value where the sign bit is set (1) and the data is 000_0000 through 111_1110, the temperature should be interpreted as 0° Celsius.

Table 8-11. Thermal Value Register Encoding

Temperature (°C)	Register Value (binary)
+127	0 111 1111
+126	0 111 1110
+100	0 110 0100
+50	0 011 0010
+25	0 001 1001
+1	0 000 0001
0	0 000 0000

8.4.6.2 Thermal Limit Registers

The SMBus thermal sensor has four Thermal Limit Registers:

- RRHL — used to read the high limit
- RRLL — used to read for the low limit
- WRHL — used to write the high limit
- WRLL — used to write the low limit

These registers allow the user to define high and low limits for the processor core thermal diode reading. The encoding for these registers is the same as for the TRR shown in Table 8-11. If the processor thermal diode reading equals or exceeds one of these limits, then the alarm bit (RHIGH or RLOW) in the Thermal Sensor Status Register is triggered.

8.4.6.3 Status Register

The Status Register shown in Table 8-12 indicates which, if any, thermal value thresholds for the processor core thermal diode have been exceeded. It also indicates whether a conversion is in progress or an open circuit has been detected in the processor core thermal diode connection. Once set, alarm bits stay set until they are cleared by a Status Register read. A successful read to the Status Register will clear any alarm bits that may have been set (unless the alarm condition persists). If the SM_ALERT# signal is enabled via the Thermal Sensor Configuration Register and a thermal diode threshold is exceeded, an alert will be sent to the platform via the SM_ALERT# signal.

This register is read by accessing the RS Command Register.

Table 8-12. SMBus Thermal Sensor Status Register

Bit	Name	Reset State	Function
7 (MSB)	BUSY	N/A	If set, indicates that the device's analog to digital converter is busy.
6	RESERVED	RESERVED	Reserved for future use
5	RESERVED	RESERVED	Reserved for future use
4	RHIGH	0	If set, indicates the processor core thermal diode high temperature alarm has activated.
3	RLOW	0	If set, indicates the processor core thermal diode low temperature alarm has activated.
2	OPEN	0	If set, indicates an open fault in the connection to the processor core diode.
1	RESERVED	RESERVED	Reserved for future use.
0 (LSB)	RESERVED	RESERVED	Reserved for future use.

8.4.6.4 Configuration Register

The Configuration Register controls the operating mode (stand-by vs. auto-convert) of the SMBus thermal sensor. Table 8-13 shows the format of the Configuration Register. If the RUN/STOP bit is set (high) then the thermal sensor immediately stops converting and enters stand-by mode. The thermal sensor will still perform analog to digital conversions in stand-by mode when it receives a one-shot command. If the RUN/STOP bit is clear (low), then the thermal sensor enters auto-conversion mode.

This register is accessed by using the thermal sensor Command Register. The RC command register is used for read commands and the WC command register is used for write commands. See Table 8-10.

Table 8-13. SMBus Thermal Sensor Configuration Register

Bit	Name	Reset State	Function
7 (MSB)	MASK	0	Mask SM_ALERT# bit. Clear the bit to allow interrupts via SM_ALERT# and allow the thermal sensor to respond to the ARA command when an alarm is active. Set the bit to disable interrupt mode. The bit is not used to clear the state of the SM_ALERT# output. An ARA command may not be recognized if the mask is enabled.
6	RUN/STOP	0	Stand-by mode control bit. If set, the device immediately stops converting, and enters stand-by mode. If cleared, the device converts in either one-shot mode or automatically updates on a timed basis.
5:0	RESERVED	RESERVED	Reserved for future use.

8.4.6.5 Conversion Rate Registers

The contents of the Conversion Rate Registers determine the nominal rate at which analog-to-digital conversions happen when the SMBus thermal sensor is in auto-convert mode. There are two Conversion Rate Registers: RCR for reading the conversion rate value; and WCR for writing the value. Table 8-14 shows the mapping between Conversion Rate Register values and the conversion rate. As indicated in Table 8-10, the Conversion Rate Register is set to its default state of 02h (0.25 Hz nominally) when the thermal sensor is powered up. There is a ±30% error tolerance between the conversion rate indicated in the conversion rate register and the actual conversion rate.

Table 8-14. SMBus Thermal Sensor Conversion Rate Registers

Register Value	Conversion Rate (Hz)
00h	0.0625
01h	0.125
02h	0.25
03h	0.5
04h	1.0
05h	2.0
06h	4.0
07h	8.0
08h to FFh	Reserved for future use

8.4.7 SMBus Thermal Sensor Alert Interrupt

The SMBus thermal sensor located on the processor includes the ability to interrupt the SMBus when a fault condition exists. The fault conditions consist of:

1. a processor thermal diode value measurement that exceeds a user-defined high or low threshold programmed into the Command Register; or
2. disconnection of the processor thermal diode from the thermal sensor.

The interrupt can be enabled and disabled via the thermal sensor Configuration Register and is delivered to the system board via the SM_ALERT# open drain output. Once latched, the SM_ALERT# should only be cleared by reading the Alert Response byte from the Alert Response Address of the thermal sensor. The Alert Response Address is a special slave address shown in Table 8-9. The SM_ALERT# will be cleared once the SMBus master device reads the slave ARA unless the fault condition persists. Reading the Status Register or setting the mask bit within the Configuration Register does not clear the interrupt.

8.4.8 SMBus Device Addressing

Of the addresses broadcast across the SMBus, the memory component claims those of the form “1010XXXZb”. The “XXX” bits are defined by pull-up and pull-down resistors on the system baseboard. These address pins are pulled down weakly (10 kW) on the processor substrate to ensure that the memory components are in a known state in systems which do not support the SMBus (or only support a partial implementation). The “Z” bit is the read/write bit for the serial bus transaction.

The thermal sensor internally decodes one of three upper address patterns from the bus of the form “0011XXXZb”, “1001XXXZb”, or “0101XXXZb”. The device’s addressing, as implemented, uses the SM_TS_A[1:0] pins in either the HI, LO, or Hi-Z state. Therefore, the thermal sensor supports nine unique addresses. To set either pin for the Hi-Z state, the pin must be left floating. As before, the “Z” bit is the read/write bit for the serial transaction.

Note that addresses of the form “0000XXXXb” are Reserved and should not be generated by an SMBus master. The thermal sensor samples and latches the SM_TS_A[1:0] signals at power-up and at the starting point of every conversion. System designers should ensure that these signals are at valid V_{IH}, V_{IL}, or floating input levels prior to or while the thermal sensor’s SM_VCC supply powers up. This should be done by pulling the pins to SM_VCC or V_{SS} via a 1 kW or smaller resistor, or leaving the pins floating to achieve the Hi-Z state. If the system designer wants to drive the SM_TS_A[1:0] pins with logic, the designer must still ensure that the pins are at valid input levels prior to or while the SM_VCC supply ramps up. The system designer must also ensure that their particular implementation does not add excessive capacitance to the address inputs. Excess capacitance at the address inputs may cause address recognition problems.

Figure 8-2 shows a logical diagram of the pin connections. Table 8-15 and Table 8-16 describe the address pin connections and how they affect the addressing of the devices.

Table 8-15. Thermal Sensor SMBus Addressing

Address (Hex)	Upper Address[1]	Device Select		8-bit Address Word on Serial Bus
		SM_TS_A1	SM_TS_A0	b[7:0]
3Xh	0011	0	0	0011000Xb
		Z[2]	0	0011001Xb
		1	0	0011010Xb
5Xh	0101	0	Z[2]	0101001Xb
		Z[2]	Z[2]	0101010Xb
		1	Z[2]	0101011Xb
9Xh	1001	0	1	1001100Xb
		Z[2]	1	1001101Xb
		1	1	1001110Xb

NOTES:
1. Upper address bits are decoded in conjunction with the device select pins.
2. A tri-state or “Z” state on this pin is achieved by leaving this pin unconnected.

Note: System management software must be aware of the processor dependent addresses for the thermal sensor.

Table 8-16. Memory Device SMBus Addressing (Sheet 1 of 2)

Address (Hex)	Upper Address[1]	Device Select			R/W
	bits 7-4	SM_EP_A2 bit 3	SM_EP_A1 bit 2	SM_EP_A0 bit 1	bit 0
A0h/A1h	1010	0	0	0	X
A2h/A3h	1010	0	0	1	X
A4h/A5h	1010	0	1	0	X

Table 8-16. Memory Device SMBus Addressing (Sheet 2 of 2)

Address (Hex)	Upper Address[1]	Device Select			R/W
	bits 7-4	SM_EP_A2 bit 3	SM_EP_A1 bit 2	SM_EP_A0 bit 1	bit 0
A6h/A7h	1010	0	1	1	X
A8h/A9h	1010	1	0	0	X
AAh/ABh	1010	1	0	1	X
ACh/ADh	1010	1	1	0	X
AEh/AFh	1010	1	1	1	X

NOTE:
1. This addressing scheme will support up to 8 processors on a single SMBus.

8.4.9 Managing Data in the PIROM

The PIROM consists of the following sections:

- Header
- Processor Data
- Processor Core Data
- Cache Data
- Package Data
- Part Number Data
- Thermal Reference Data
- Feature Data
- Other Data

Details on each of these sections are described below.

Note: Reserved fields or bits SHOULD be programmed to zeros. However, OEMs should not rely on this model.

8.4.9.1 Header

To maintain backward compatibility, the Header defines the starting address for each subsequent section of the PIROM. Software should check for the offset before reading data from a particular section of the ROM.

Example: Code looking for the cache data of a processor would read offset 05h to find a value of 25h. 25h is the first address within the 'Cache Data' section of the PIROM.

The Header also includes the data format revision at offset 0h and the EEPROM size (formatted in hex bytes) at offset 01-02h. The data format revision is used whenever fields within the PIROM are redefined. Normally the revision would begin at a value of 1. If a field, or bit assignment within a field, is changed such that software needs to discern between the old and new definition, then the data format revision field should be incremented.

The EEPROM size provides the size of the PIROM in hex bytes. The PIROM is 128 bytes; thus, offset 01 - 02h would be programmed to 80h.

8.4.9.2 Processor Data

This section contains two pieces of data:

- The S-spec/QDF of the part in ASCII format
- (1) 2-bit field to declare if the part is a pre-production sample or a production unit

The S-spec/QDF field is six ASCII characters wide and is programmed with the same S-spec/QDF value as marked on the processor. If the value is less than six characters in length, leading spaces (20h) are programmed in this field.

Example: A processor with a QDF mark of QEU5 contains the following in field 0E-13h: 20, 20, 51, 45, 55, 35h. This data consists of two blanks at 0Eh and 0Fh followed by the ASCII codes for QEU5 in locations 10 - 13h.

Offset 14h contains the sample/production field, which is a two-bit field and is LSB aligned. All Q-spec material will use a value of 00b. All S-spec material will use a value of 01b. All other values are reserved.

Example: A processor with a Qxxx mark (engineering sample) will have offset 14h set to 00b. A processor with an Sxxxx mark (production unit) will use 01b at offset 14h.

8.4.9.3 Processor Core Data

This section contains core silicon-related data.

8.4.9.3.1 CPUID

The CPUID field is a copy of the results in EAX[13:0] from Function 1 of the CPUID instruction.

Note: The field is not aligned on a byte boundary since the first two bits of the offset are reserved. Thus, the data must be shifted right by two in order to obtain the same results.

Example: The CPUID of a C-0 stepping 64-bit Intel® Xeon™ processor MP with up to 8MB L3 cache is 0F41h. The value programmed into offset 16 - 17h of the PIROM is 3D04h.

Note: The first two bits of the PIROM are reserved, as highlighted in the example below.

CPUID instruction results	0000	1111	0100	0001 (0F41h)
PIROM content	0011	1101	0000	01**00** (3D04h)

8.4.9.3.2 Front Side Bus Frequency

Offset 1A - 1Bh provides front side bus frequency information. Systems may need to read this offset to decide if all installed processors support the same front side bus speed. Because the Intel NetBurst microarchitecture bus is described as a 4X data bus, the frequency given in this field is currently 667 MHz. The data provided is the speed, rounded to a whole number, and reflected in hex.

Example: The processor supports a 667 MHz front side bus. Therefore, offset 1A - 1Bh has a value of 029Bh.

8.4.9.3.3 Multi-Processor Support

Offset 1Ch has 2 bits defined for representing the supported number of physical processors on the bus. These two bits are MSB aligned where 00b equates to single-processor operation, 01b is a dual-processor operation, and 11b represents multi-processor operation. Normally, only values of 01 and 11b are used. The remaining six bits in this field are reserved for the future use.

8.4.9.3.4 Maximum Core Frequency

Offset 1D - 1Eh provides the maximum core frequency for the processor. The frequency should equate to the markings on the processor and/or the QDF/S-spec speed even if the parts are not limited or locked to the intended speed. Format of this field is in MHz, rounded to a whole number, and encoded in hex format.

Example: A 3.00 GHz processor will have a value of 0BB8h, which equates to 3000 decimal.

8.4.9.3.5 Core Voltage

There are two areas defined in the PIROM for the core voltages associated with the processor. Offset 1F - 20h is the Processor Core VID (Voltage Identification) field and contains the voltage requested via the VID pins. In the case of the 64-bit Intel® Xeon™ processor MP with up to 8MB L3 cache, this is 1.3875 V. This field, rounded to the next thousandth, is in mV and is reflected in hex. This data is also in Table 2-9. Some systems read this offset to determine if all processors support the same default VID setting.

Minimum core voltage is reflected in offset 21 - 22h. This field is in mV and reflected in hex. The minimum V_{CC} reflected in this field is the minimum allowable voltage assuming the FMB maximum current draw.

Note: The minimum core voltage value in offset 21 - 22h is a single value that assumes the FMB maximum current draw. Refer to Table 2-10 for the minimum core voltage specifications based on actual real-time current draw.

Example: The specifications for a 64-bit Intel® Xeon™ processor MP with up to 8MB L3 cache at FMB are 1.3875 V VID and 1.229 V minimum voltage. Offset 1F - 20h would contain 056Ch (1388 decimal) and offset 21 - 22h would contain 04D2h (1234 decimal).

8.4.9.3.6 T_{CASE} Maximum

The last field within Processor Core Data is the T_{CASE} Maximum field. The field reflects temperature in degrees Celsius in hex format. This data can be found in the Table 7-1. The thermal specifications are specified at the case (IHS).

8.4.9.4 Cache Data

This section contains cache-related data.

8.4.9.4.7 L2/L3 Cache Size

Offset 27 - 28h is the L2 cache size field. The field reflects the size of the level two cache in kilobytes. Offset 29 - 3Ah is the L3 cache size field and also reflects size in kilobytes. Both fields are in hex format.

Example: The 64-bit Intel® Xeon™ processor MP with up to 8MB L3 cache has a 1 MB (1024 KB) L2 cache and either 4 MB (4096 KB) or 8 MB (8192 KB) L3 cache. Thus, offset 27 - 28h will contain 0400h, and offset 29 - 2Ah will contain 1000h (for 4 MB) or 2000h (for 8 MB).

8.4.9.4.8 Cache Voltage

There are two areas defined in the PIROM for the L3 cache voltages associated with the processor. Offset 2B - 2Ch is the Processor Cache VID (Cache Voltage Identification), or CVID, field and contains the voltage requested via the CVID pins. In the case of the 64-bit Intel® Xeon™ processor MP with up to 8MB L3 cache, this is 1.275 V. This field is in mV and is reflected in hex. This data is also in Table 2-9. Some systems read this offset to determine if all processors support the same default CVID setting.

Minimum L3 cache voltage specifications are reflected in offset 2D - 2Eh. This field is in mV and reflected in hex. This data is also in Table 2-9. For processors that follow a load line DC specification, the minimum V_{CACHE} reflected in this field should reflect the minimum allowable voltage at maximum current.

Example: The specifications for a 64-bit Intel® Xeon™ processor MP with up to 8MB L3 cache are 1.275 V CVID and 1.125 V minimum voltage (at maximum current). Offset 2B - 2Ch would contain 04FBh (1275 decimal) and offset 2D - 2Eh would contain 0465h (1125 decimal).

8.4.9.5 Package Data

This section describes the package revision location at offset 32 - 35h. This field tracks the highest level revision. It is provided in ASCII format of four characters (8 bits x 4 characters = 32 bits). The package is documented as 1.0, 2.0, etc. Because this only consumes three ASCII characters, a leading space is provided in the data field.

Example: The C-0 stepping of the 64-bit Intel® Xeon™ processor MP with up to 8MB L3 cache utilizes revision 1.0 of the FC-mPGA package. Thus, at offset 32-35h, the data is a space followed by 1.0. In hex, this would be 20, 31, 2E, 30.

8.4.9.6 Part Number Data

This section provides traceability. There are 208 available bytes in this section for future use.

8.4.9.6.9 Processor Part Number

Offset 38 - 3Eh contains seven ASCII characters reflecting the Intel part number for the processor. This information is typically marked on the outside of the processor. If the part number is less than 7 characters, a leading space is inserted into the value. The part number should match the information found in the marking specification found in Section 4.

Example: A processor with a part number of 80546KF will have data found at offset 38 - 3Eh is 38, 30, 35, 34, 36, 4B, 46.

8.4.9.6.10 Processor Electronic Signature

Offset 4D - 54h contains a 64-bit identification number. Intel does not guarantee that each processor will have a unique value in this field.

8.4.9.7 Feature Data

This section provides information on key features that the platform may need to understand without powering on the processor.

8.4.9.7.11 Processor Core Feature Flags

Offset 74 - 77h contains a copy of results in EDX[31:0] from Function 1 of the CPUID instruction. These details provide instruction and feature support by product family. A decode of these bits is found in the *AP-485 Intel® Processor Identification and CPUID Instruction* application note.

8.4.9.7.12 Processor Feature Flags

Offset 78h provides additional feature information from the processor. This field is defined as follows:

Table 8-17. Offset 78h Definitions

Bit	Definition
7	Reserved
6	Serial signature (set if there is a serial signature at offset 4D - 54h)
5	Electronic signature present (set if there is a electronic signature at 4D - 54h)
4	Thermal Sense Device present (set if an SMBus thermal sensor on package)
3	Reserved
2	OEM EEPROM present (set if there is a scratch ROM at offset 80 - FFh)
1	Core VID present (set if there is a VID provided by the processor)
0	L3 Cache present (set if there is a level 3 cache on the processor)

8.4.9.7.13 Additional Processor Feature Flags

All bits of this field are reserved at this time. The field resides at offset 79 - 7Bh.

8.4.9.8 Other Data

Addresses 7E - 7F are listed as reserved.

8.4.9.9 Checksums

The PIROM includes multiple checksums. Table 8-18 includes the checksum values for each section defined in the 128 byte ROM, except Other Data.

Table 8-18. 128 Byte ROM Checksum Values

Section	Checksum Address
Header	0Dh
Processor Data	15h
Processor Core Data	24h
Cache Data	31h
Package Data	37h
Part Number Data	6Fh
Feature Data	7Dh
Other Data	None Defined

Checksums are automatically calculated and programmed by Intel. The first step in calculating the checksum is to add each byte from the field to the next subsequent byte. This result is then negated to provide the checksum.

Example: For a byte string of AA445Ch, the resulting checksum will be B6h.

AA = 10101010 44 = 01000100 5C = 0101100

AA + 44 + 5C = 01001010

Negate the sum: 10110101 +1 = **101101 (B6h)**

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9 Boxed Processor Specifications

9.1 Introduction

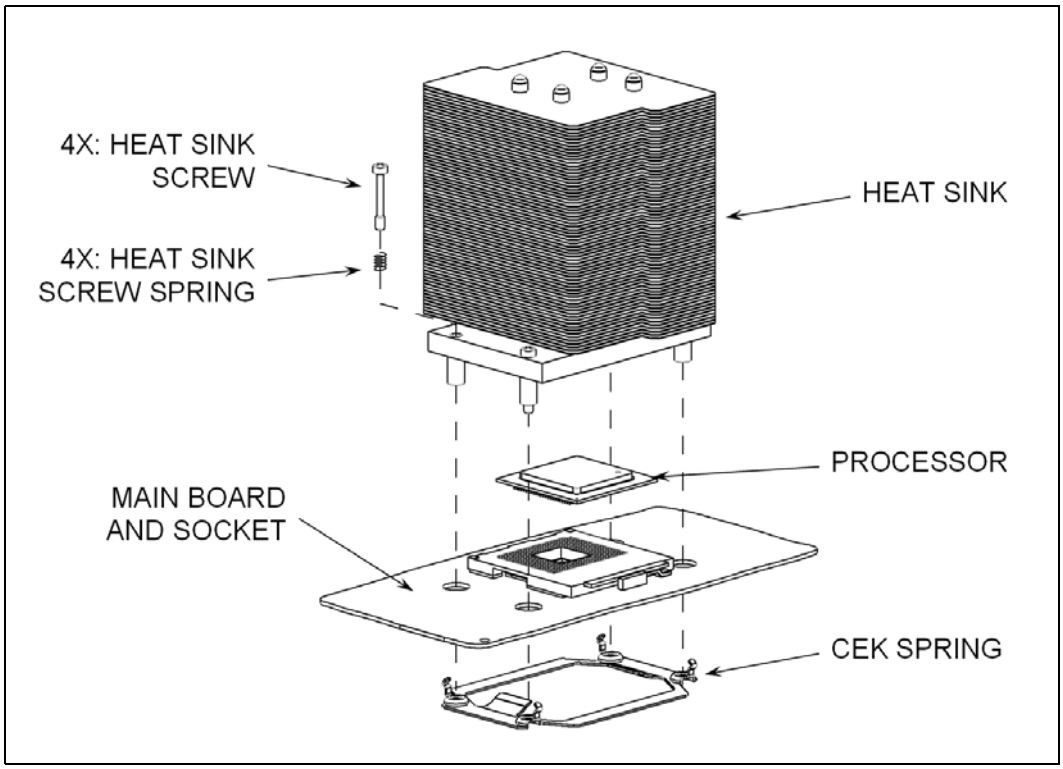
The 64-bit Intel® Xeon™ processor MP with up to 8MB L3 cache processor may also be offered as an Intel boxed processor. Intel boxed processors are intended for system integrators who build systems from components available through distribution channels. The boxed thermal solution is still under development and subject to change. This section is meant to provide some insight into the current direction of the thermal solution. Future revisions may have solutions that differ from those discussed here.

The current thermal solution plan for the boxed 64-bit Intel® Xeon™ processor MP with up to 8MB L3 cache processor is to include an unattached passive heatsink. This solution is currently targeted at chassis which are 3U and above in height.

This section documents baseboard and platform requirements for the thermal solution, supplied with the boxed 64-bit Intel® Xeon™ processor MP with up to 8MB L3 cache processor. This section is particularly important to companies that design and manufacture baseboards, chassis and complete systems. Figure 9-1 shows the conceptual drawing of the boxed processor thermal solution.

Drawings in this section reflect only the specifications on the Intel boxed processor product. These dimensions should not be used as a generic keep-out zone for all cooling solutions. It is the system designer’s responsibility to consider their proprietary cooling solution when designing to the required keep-out zone on their system platform and chassis.

Figure 9-1. Passive Processor Thermal Solution (3U and larger)



NOTE:
1. The heatsink in this image is for reference only.
2. This drawing shows the retention scheme for the boxed processor.

9.2 Mechanical Specifications

This section documents the mechanical specifications of the boxed processor passive heatsink.

9.2.1 Boxed Processor Heatsink Dimensions

The boxed processor is shipped with an unattached passive heatsink. Clearance is required around the heatsink to ensure unimpeded airflow for proper cooling. The physical space requirements and dimensions for the boxed processor and assembled heatsink are shown in the following figures.

Figure 9-2. Top Side Board Keep-Out Zones (Part 1)

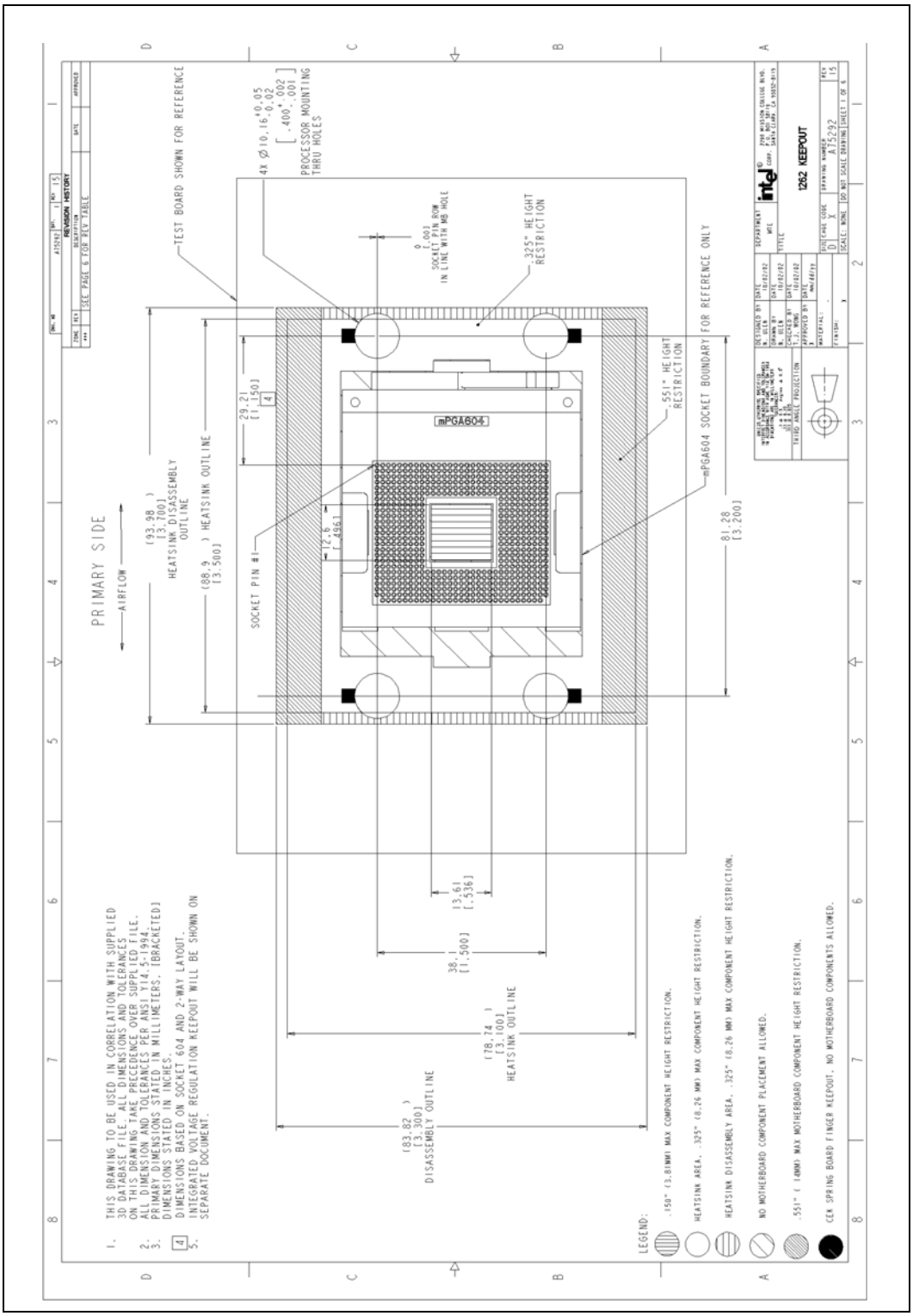


Figure 9-3. Top Side Board Keep-Out Zones (Part 2)

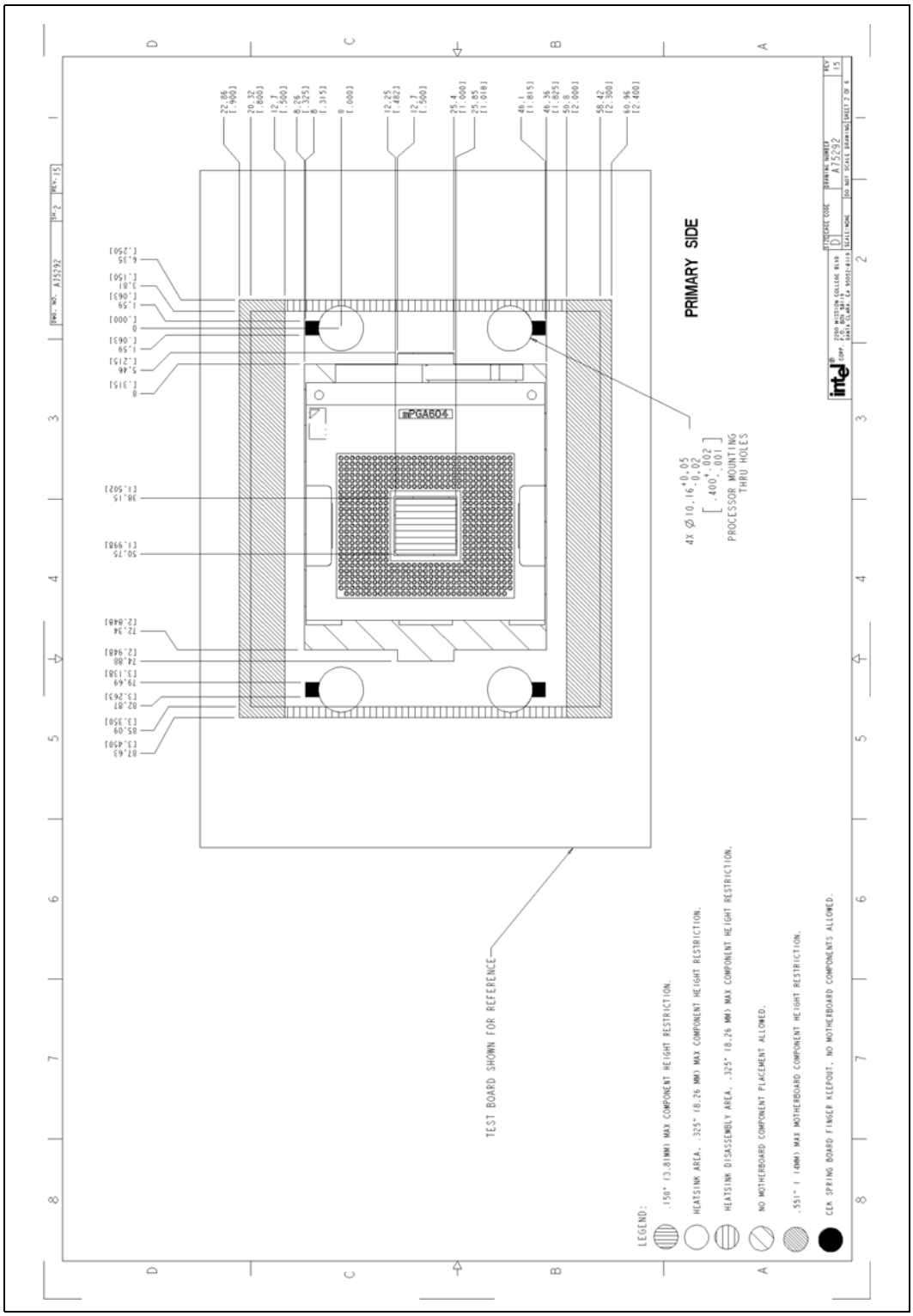


Figure 9-4. Bottom Side Board Keep-Out Zones

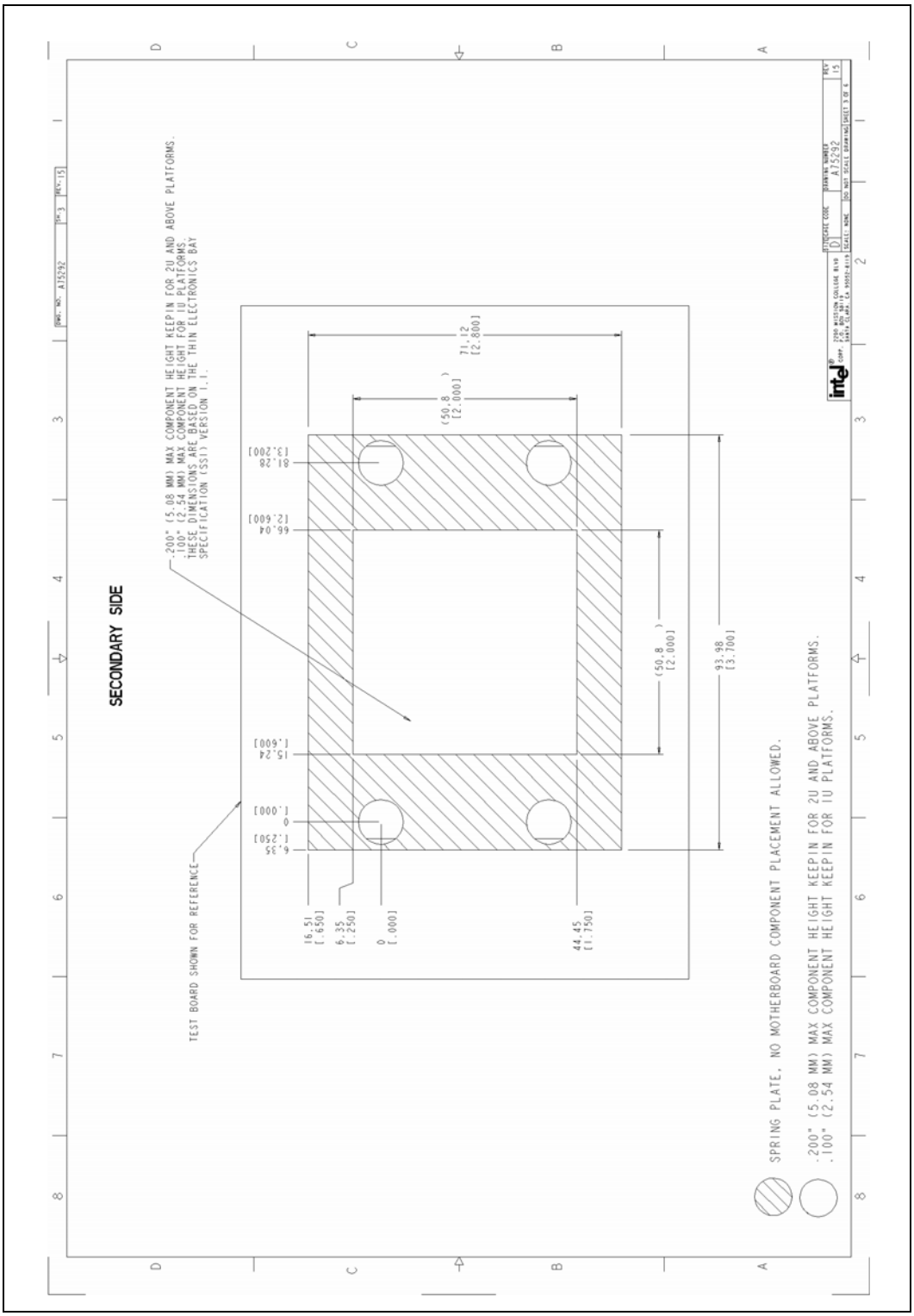


Figure 9-5. Board Mounting-Hole Keep-Out Zones

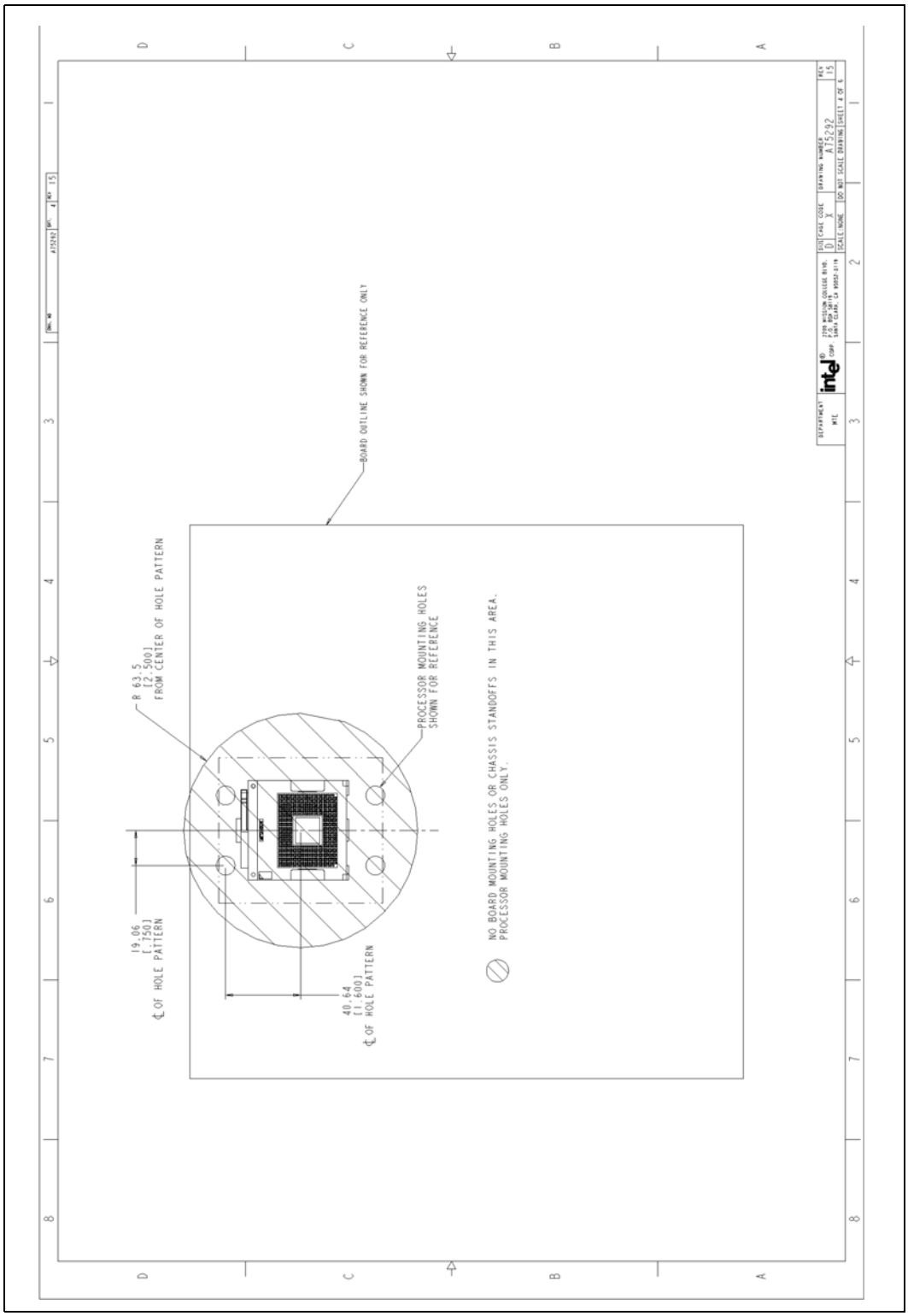


Figure 9-6. Thermal Solution Volumetric

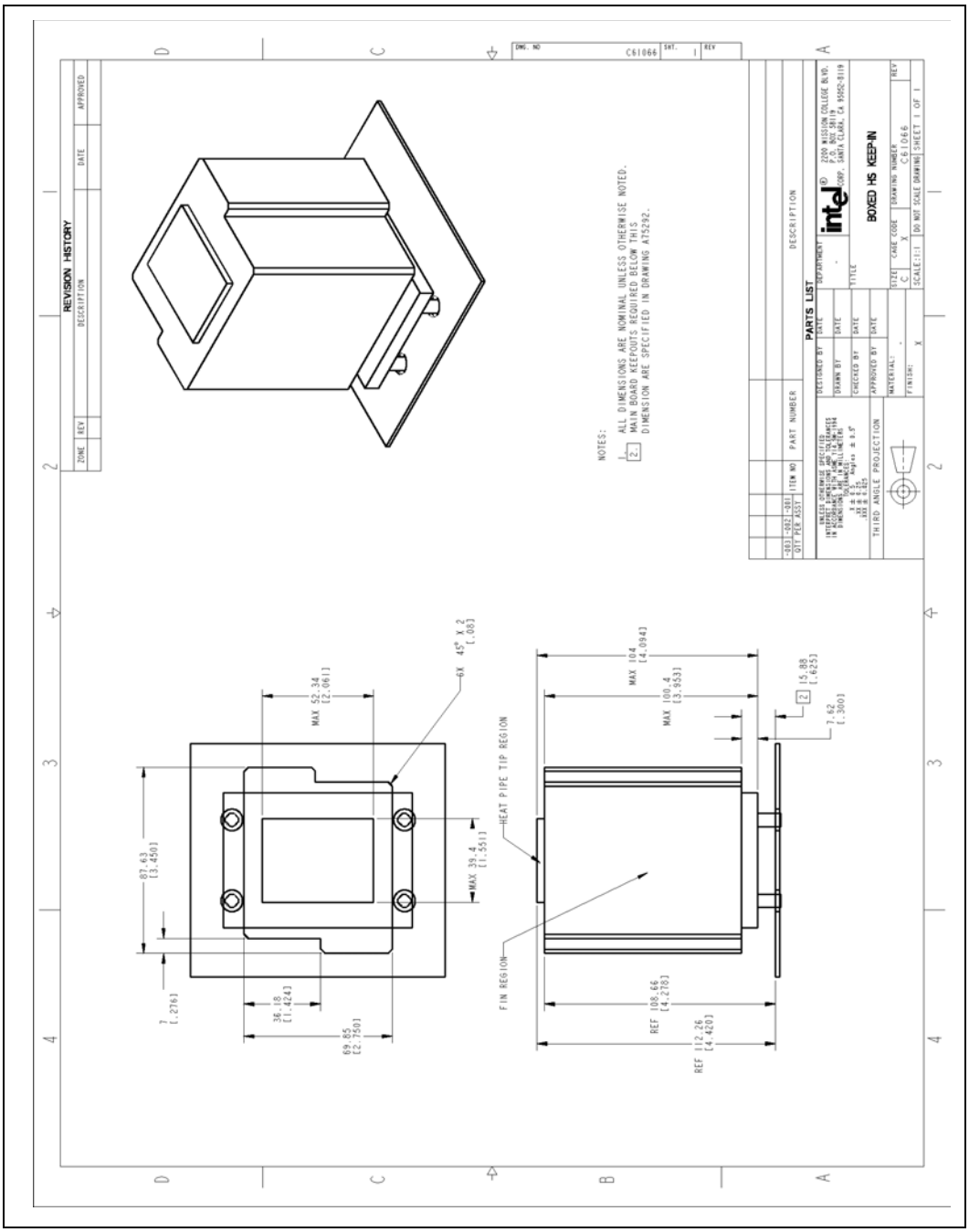
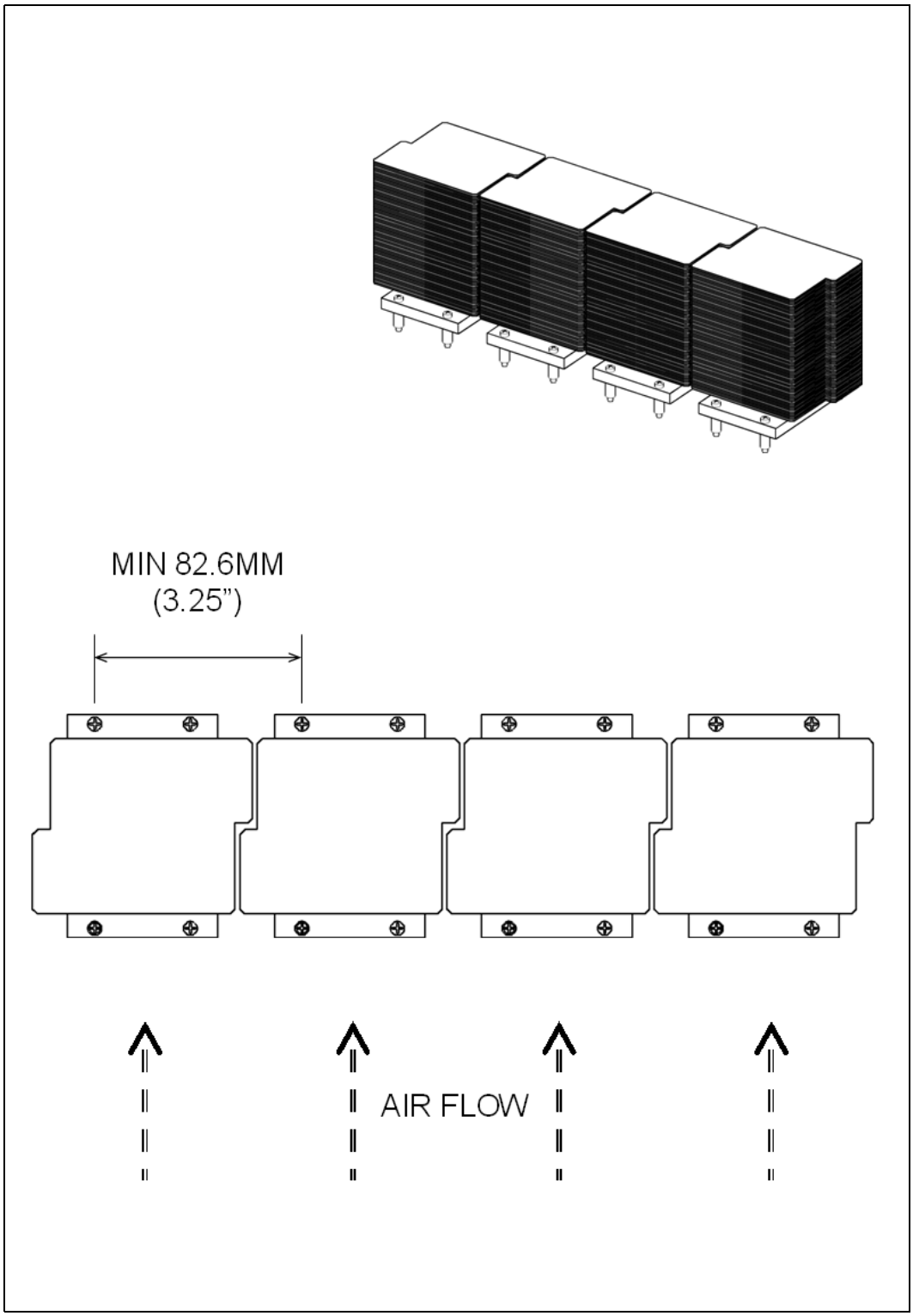


Figure 9-7. Recommended Processor Layout and Pitch



9.2.2 Boxed Processor Heatsink Weight

The boxed processor heatsink weight is approximately 530 grams. See Section 4 of this document for details on the processor weight.

9.2.3 Boxed Processor Retention Mechanism and Heatsink Supports

Baseboards and chassis's designed for use by system integrators should include holes that are in proper alignment with each other to support the boxed processor. See Figure 9-7 for example of processor pitch and layout.

Figure 9-1 illustrates the new retention solution. This is designed to extend air-cooling capability through the use of larger heatsinks with minimal airflow blockage and minimal bypass. These retention mechanisms can allow the use of much heavier heatsink masses compared to legacy solution limitations by using a load path attached to the chassis pan. The cooling solution spring (Figure 9-1 labeled as "CEK SPRING") on the under side of the baseboard provides the necessary compressive load for the thermal interface material. The baseboard is intended to be isolated such that the dynamic loads from the heatsink are transferred to the chassis pan via the heatsink screws and heatsink standoffs. This reduces the risk of package pullout and solder joint failures in a shock and vibe situation.

The assembly requires larger diameter holes to compensate for the cooling solution spring embosses. See Figure 9-2 and Figure 9-3 for processor mounting through holes.

9.3 Thermal Specifications

This section describes the cooling requirements of the heatsink solution utilized by the boxed processor.

9.3.1 Boxed Processor Cooling Requirements

The boxed processor will be cooled by forcing ducted chassis fan airflow through the passive heat sink solution. Meeting the processor's temperature specifications is a function of the thermal design of the entire system, and ultimately the responsibility of the system integrator. The processor temperature specification is found in Section 7 of this document. For the boxed processor passive heatsink to operate properly, chassis air movement devices are required. Necessary airflow and associated flow impedance is 29 cfm at 0.10" H_2O.

In addition, the processor pitch should be 3.25 inches, or slightly more, when placed in side by side orientation. Figure 9-7 illustrates the side by side orientation and pitch. Note that the heatsinks are interleaved to reduce air bypass.

It is also recommended that the ambient air temperature outside of the chassis be kept at or below 35°C. The air passing directly over the processor heatsink should not be preheated by other system components (such as another processor), and should be kept at or below 40°C. Again, meeting the processor's temperature specification is the responsibility of the system integrator.

9.3.2 Boxed Processor Contents

The boxed processor will include the following items:

- 64-bit Intel® Xeon™ processor MP with up to 8MB L3 cache processor
- Unattached Passive Heatsink with captive screws
- Thermal Interface Material (pre-attached)
- Warranty / Installation manual with Intel Inside logo

The other items listed in Figure 9-1, required with this thermal solution should be shipped with either the chassis or the mainboard. They include:

- Cooling Solution Spring (typically included with mainboard)
- Chassis Standoffs
- System fans

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10 Debug Tools Specifications

10.1 Logic Analyzer Interface (LAI)

Intel is working with two logic analyzer vendors to provide logic analyzer interfaces (LAIs) for use in debugging systems. Tektronix and Agilent should be contacted to get specific information about their logic analyzer interfaces. The following information is general in nature. Specific information must be obtained from the logic analyzer vendor.

Due to the complexity of multiprocessor systems, the LAI is critical in providing the ability to probe and capture front side bus signals. There are two sets of considerations to keep in mind when designing systems that can make use of an LAI: mechanical and electrical.

10.1.1 Mechanical Considerations

The LAI is installed between the processor socket and the processor. The LAI pins plug into the socket, while the processor pins plug into a socket on the LAI. Cabling that is part of the LAI egresses the system to allow an electrical connection between the processor and a logic analyzer. The maximum volume occupied by the LAI, known as the keepout volume, as well as the cable egress restrictions, should be obtained from the logic analyzer vendor. System designers must make sure that the keepout volume remains unobstructed inside the system. Note that it is possible that the keepout volume reserved for the LAI may differ from the space normally occupied by the processor heatsink. If this is the case, the logic analyzer vendor will provide a cooling solution as part of the LAI.

10.1.2 Electrical Considerations

The LAI will also affect the electrical performance of the front side bus; therefore, it is critical to obtain electrical load models from each of the logic analyzer vendors to be able to run system level simulations to prove that their tool will work in the system. Contact the logic analyzer vendor for electrical specifications and load models for the LAI solution they provide.

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